



MS-7501 VER:3.0

CPU:

AMD M2 Athlon 64/Athlon 64 FX AM2R2

System Chipset:

AMD/ATI RS780

AMD/ATI SB700

On Board Chipset:

FINTEK Super I/O -- F71882

LAN -- RTL8111C/RTL8101E

HD Codec -- ALC888S-VC

BIOS -- SPI ROM 8M

1394 -- JMB381

Main Memory:

DDR II X 4 (Max 8GB)

Expansion Slots:

PCI-E X 16 *1

PCI-E X 1 *1

PCI 2.2 Slot X 2

Clock Generator:

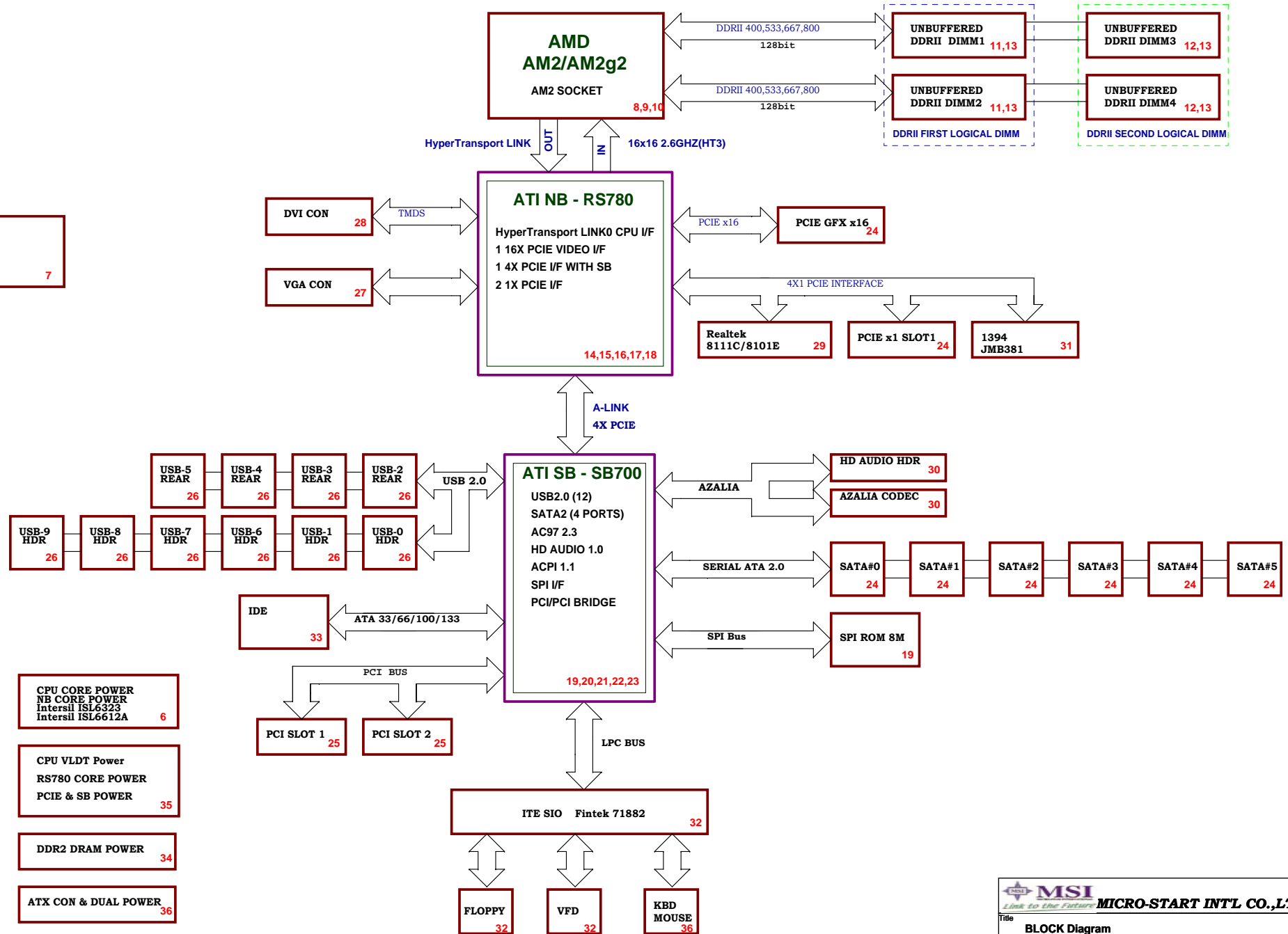
Controller--ICS9LPRS477

PWM:

Controller -- ST6740L + UP6262 4+1 Phase

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Project RS-780 BLOCK DIAGRAM



SB700 GPIO Config

GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
RI#/EXTENTVNT0#		RI#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SMI#/EXTENTVNT1#		LPC_SMI#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTRIP#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

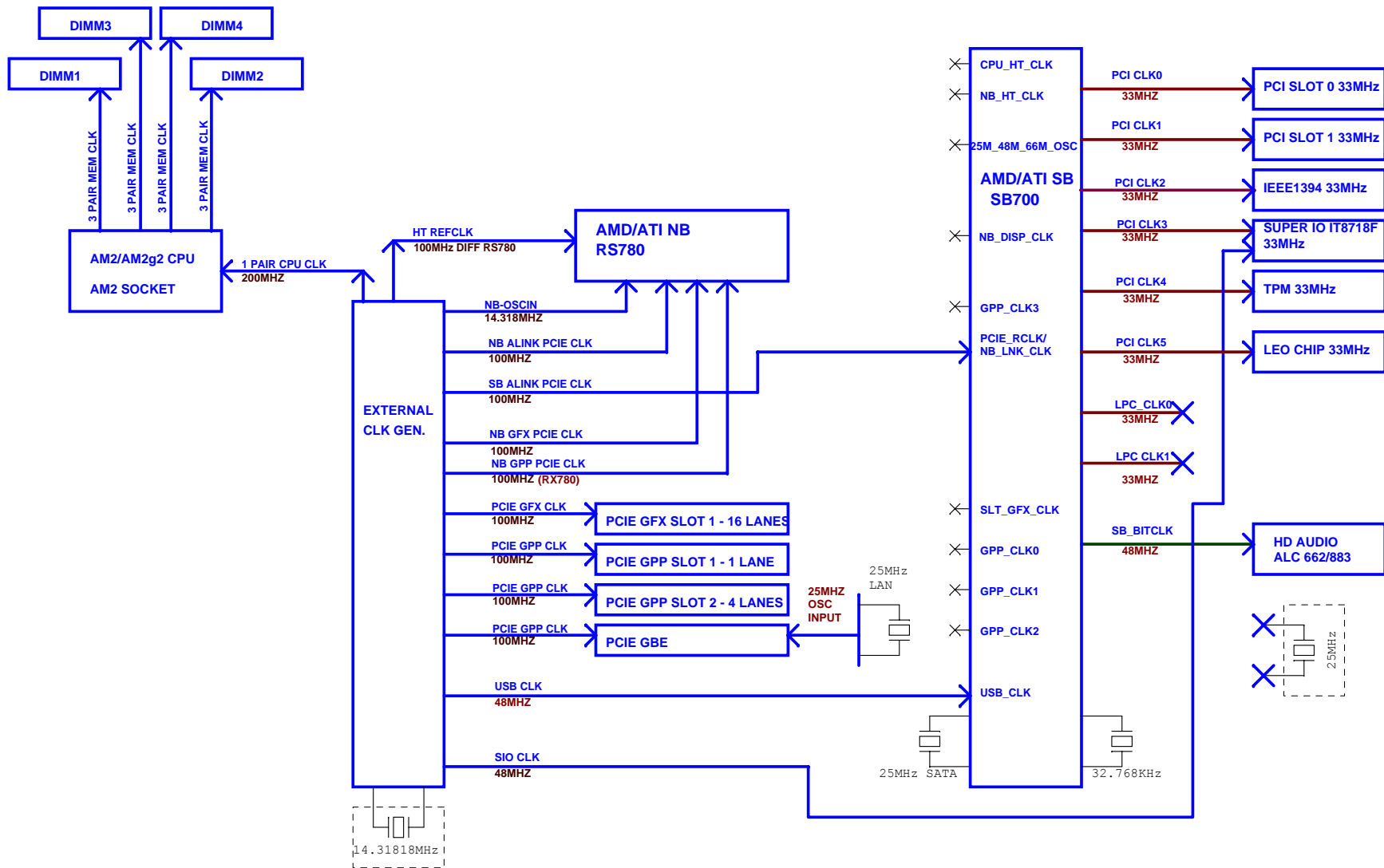
GPIO Name	Type	Function Description	Pin	Page
IDE_D4/GPIO19		Unused	AD21	19
IDE_D5/GPIO20		Unused	AE20	19
IDE_D6/GPIO21		Unused	AB20	19
IDE_D7/GPIO22		Unused	AD19	19
IDE_D8/GPIO23		Unused	AE19	19
IDE_D9/GPIO24		Unused	AC20	19
IDE_D10/GPIO25		Unused	AD20	19
IDE_D11/GPIO26		Unused	AE21	19
IDE_D12/GPIO27		Unused	AB22	19
IDE_D13/GPIO28		Unused	AD22	19
IDE_D14/GPIO29		Unused	AE23	19
IDE_D15/GPIO30		Unused	AC23	19
SPI_DI/GPIO12		SPI_DATAIN	G6	19
SPI_DO/GPIO11		SPI_DATAOUT	D2	19
SPI_CLK/GPIO47		SPI_CLK	D1	19
SPI_HOLD#/GPIO31		SPI_HOLD_L	F4	19
SPI_CS#/GPIO32		SPI_CS#	F3	19
LAN_RST#/GPIO13		CPU_PRESENT#	U15	19
ROM_RST#/GPIO14		Unused	J1	19
FANOUT0/GPIO3		Unused	M8	19
FANOUT1/GPIO48		COM_GPIO	M5	19
FANOUT2/GPIO49		Unused	M7	19
FANIN0/GPIO50		Unused	P5	19
FANIN1/GPIO51		Unused	P8	19
FANIN2/GPIO52		Unused	E8	19
TEMPIN0/GPIO61		Unused	B6	19
TEMPIN1/GPIO62		Unused	A6	19
TEMPIN2/GPIO63		Unused	A5	19
TEMPIN3/TALERT#/GPIO64		TALERT#	B5	19
VIN0/GPIO53		BIOS_WP#1	A4	19
VIN1/GPIO54		BIOS_WP#2	B4	19
VIN2/GPIO55		CLR_COMS	C4	19
VIN3/GPIO56		LAN_DISABLE	D4	19
VIN4/GPIO57		Unused	D5	19
VIN5/GPIO58		Unused	D6	19
VIN6/GPIO59		Unused	A7	19
VIN7/GPIO60		Unused	B7	19

Super I/O GPIO Config

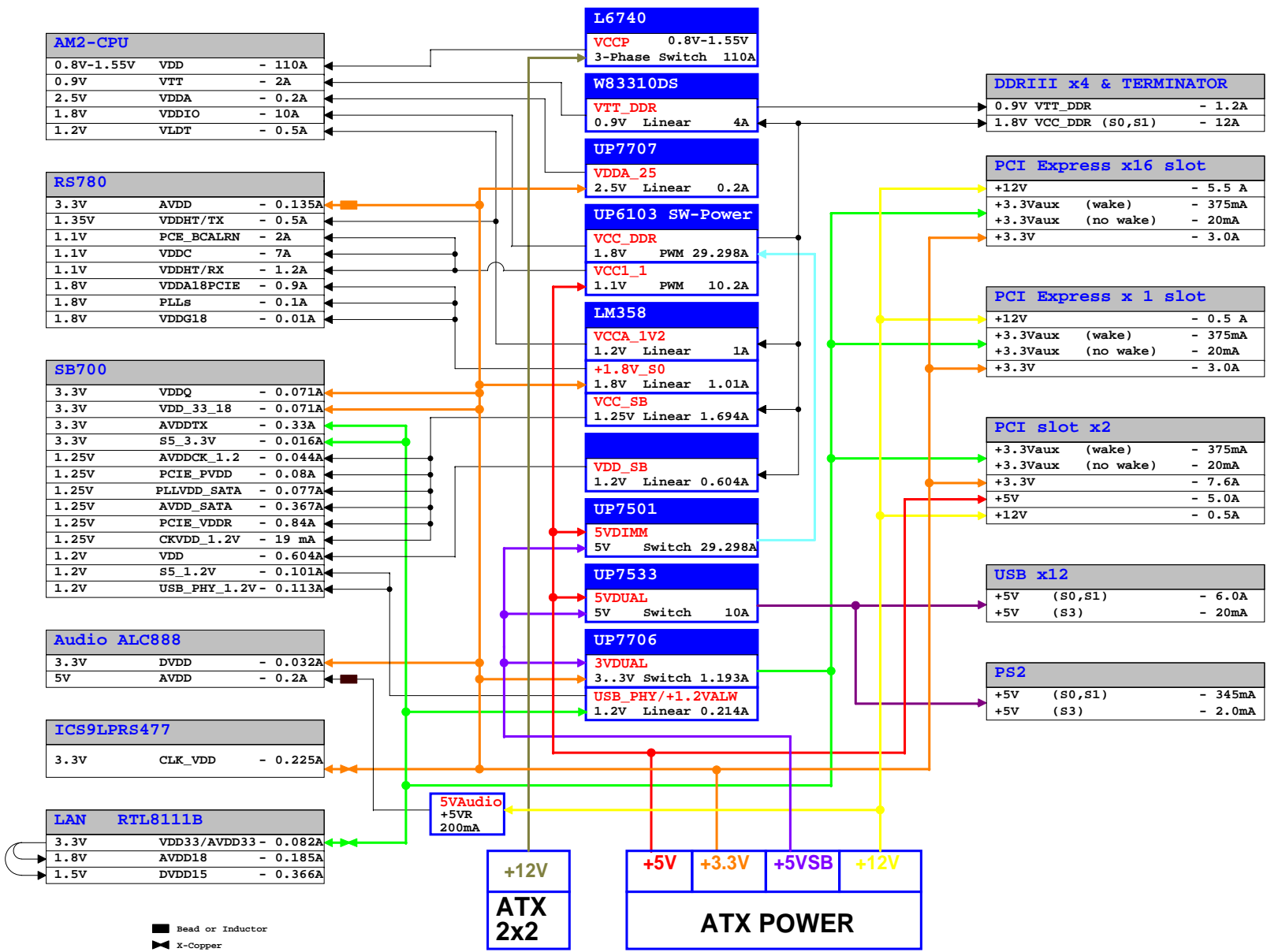
GPIO Name	Type	Function Description	Pin	Page
VID05/GP27		LEO_GPIO2	20	26
VID04/GP26		LEO_GPIO1	21	26
VID01/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SMI#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

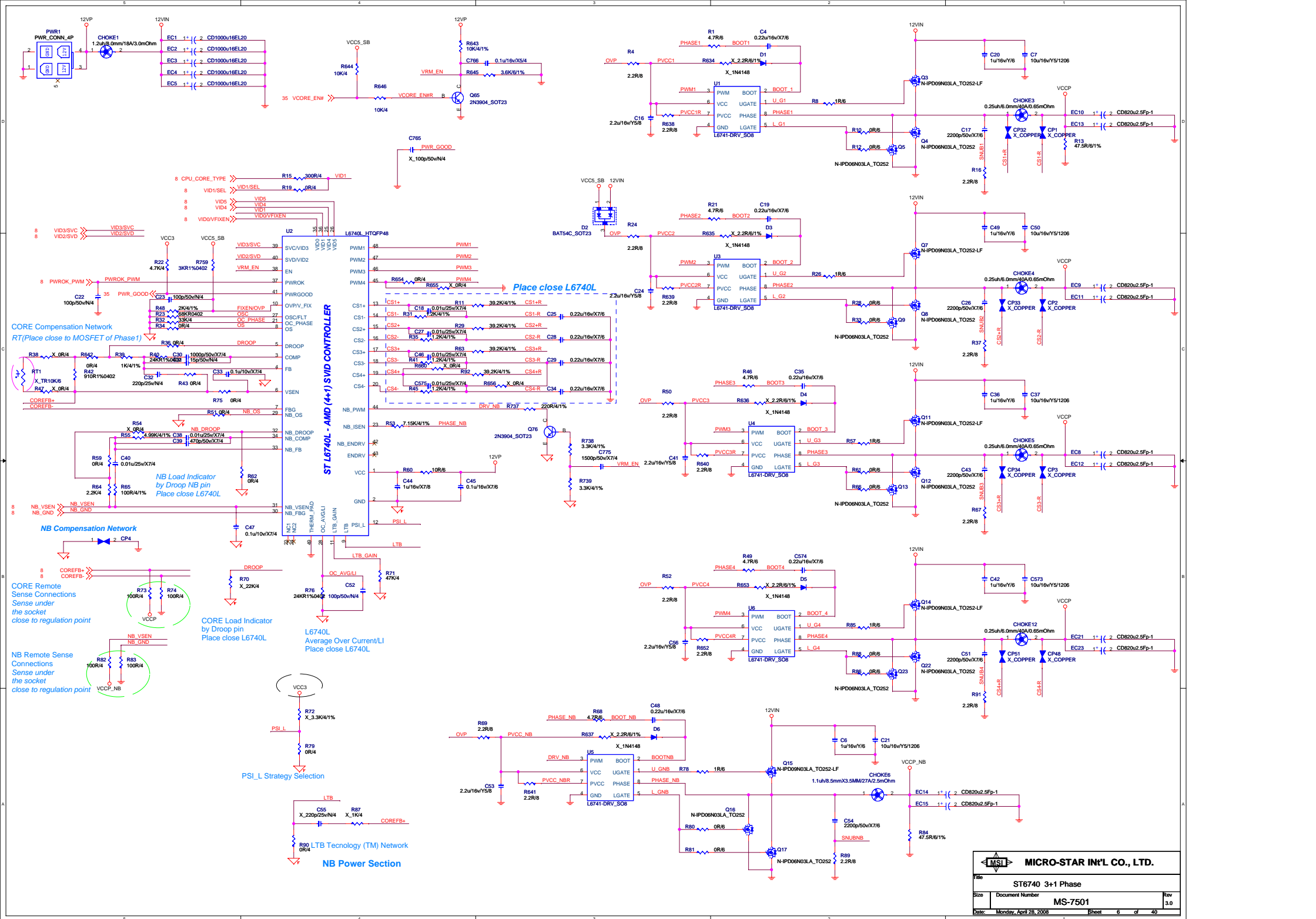
PCI Config.

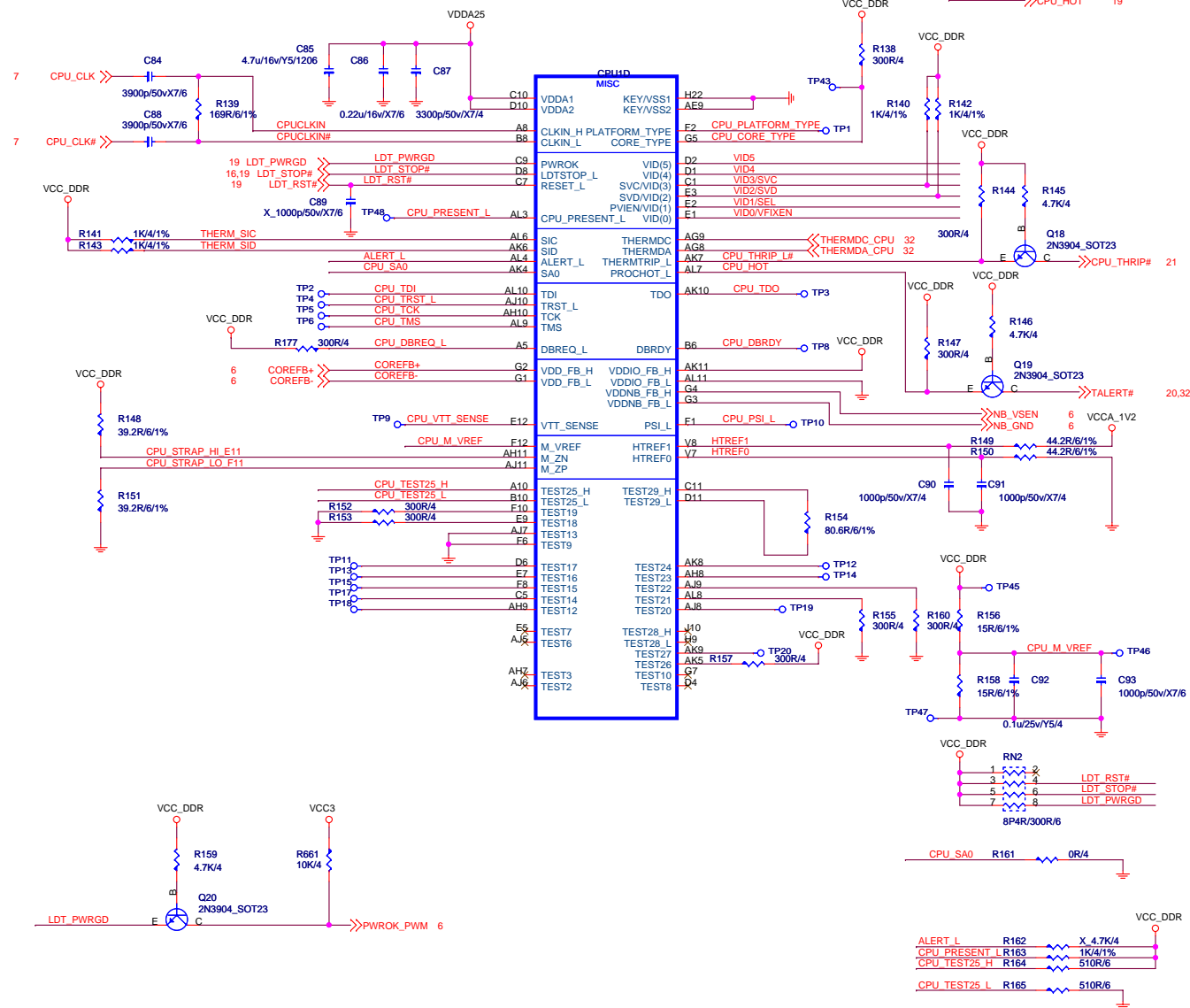
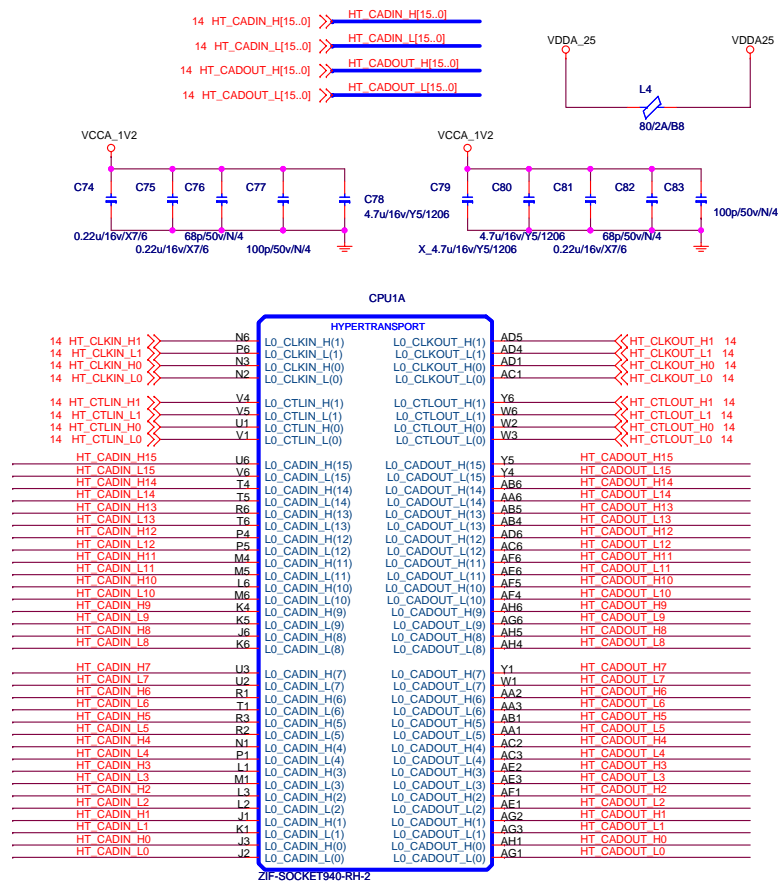
DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTE# PCI_INTF# PCI_INTG# PCI_INTH#	PREQ#0 PGNT#0	AD18	PCICLK0
PCI Slot 2	PCI_INTF# PCI_INTG# PCI_INTH# PCI_INTE#	PREQ#1 PGNT#1	AD19	PCICLK1
PCI Slot 1	PCI_INTG# PCI_INTH# PCI_INTE# PCI_INTF#	PREQ#2 PGNT#2	AD17	PCICLK2



Power Deliver Chart







11,12 MEM_MA_DQS_L[7..0] >> MEM_MA_DQS_L[7..0]
11,12 MEM_MA_DQS_H[7..0] >> MEM_MA_DQS_H[7..0]
11,12 MEM_MA_DM[7..0] >> MEM_MA_DM[7..0]
11,12,13 MEM_MA_ADD[15..0] >> MEM_MA_ADD[15..0]
11,12 MEM_MA_DATA[63..0] >> MEM_MA_DATA[63..0]

11,12 MEM_MB_DQS_L[7..0] >> MEM_MB_DQS_L[7..0]
11,12 MEM_MB_DQS_H[7..0] >> MEM_MB_DQS_H[7..0]
11,12 MEM_MB_DM[7..0] >> MEM_MB_DM[7..0]
11,12,13 MEM_MB_ADD[15..0] >> MEM_MB_ADD[15..0]
11,12 MEM_MB_DATA[63..0] >> MEM_MB_DATA[63..0]

CPU1B

MEMORY INTERFACE A

11,13 MEM_MA0_CLK_H2 >> MEM_MA0_CLK_H2 AG21
11,13 MEM_MA0_CLK_L2 >> MEM_MA0_CLK_L2 AG20
11,13 MEM_MA0_CLK_H1 >> MEM_MA0_CLK_H1 G19
11,13 MEM_MA0_CLK_L1 >> MEM_MA0_CLK_L1 H19
11,13 MEM_MA0_CLK_H0 >> MEM_MA0_CLK_H0 U27
11,13 MEM_MA0_CLK_L0 >> MEM_MA0_CLK_L0 U26
11,13 MEM_MA0_CS_L1 >> MEM_MA0_CS_L1 AC25
11,13 MEM_MA0_CS_L0 >> MEM_MA0_CS_L0 AA24
11,13 MEM_MA0_ODT0 >> MEM_MA0_ODT0 AC28
12,13 MEM_MA1_CLK_H2 >> MEM_MA1_CLK_H2 AE20
12,13 MEM_MA1_CLK_L2 >> MEM_MA1_CLK_L2 AE19
12,13 MEM_MA1_CLK_H1 >> MEM_MA1_CLK_H1 G20
12,13 MEM_MA1_CLK_L1 >> MEM_MA1_CLK_L1 G21
12,13 MEM_MA1_CLK_H0 >> MEM_MA1_CLK_H0 V27
12,13 MEM_MA1_CLK_L0 >> MEM_MA1_CLK_L0 W27
12,13 MEM_MA1_CS_L1 >> MEM_MA1_CS_L1 AD27
12,13 MEM_MA1_CS_L0 >> MEM_MA1_CS_L0 AA25
12,13 MEM_MA1_ODT0 >> MEM_MA1_ODT0 AC27
11,12,13 MEM_MA_CAS_L >> MEM_MA_CAS_L AB25
11,12,13 MEM_MA_WE_L >> MEM_MA_WE_L AB27
11,12,13 MEM_MA_RAS_L >> MEM_MA_RAS_L AA26
11,12,13 MEM_MA_BANK2 >> MEM_MA_BANK2 N25
11,12,13 MEM_MA_BANK1 >> MEM_MA_BANK1 Y27
11,12,13 MEM_MA_BANK0 >> MEM_MA_BANK0 AA27
12,13 MEM_MA_CKE1 >> MEM_MA_CKE1 L27
11,13 MEM_MA_CKE0 >> MEM_MA_CKE0 M25
MEM_MA_ADD15 >> MEM_MA_ADD15 M27
MEM_MA_ADD14 >> MEM_MA_ADD14 N24
MEM_MA_ADD13 >> MEM_MA_ADD13 AC26
MEM_MA_ADD12 >> MEM_MA_ADD12 N26
MEM_MA_ADD11 >> MEM_MA_ADD11 P25
MEM_MA_ADD10 >> MEM_MA_ADD10 Y25
MEM_MA_ADD9 >> MEM_MA_ADD9 N27
MEM_MA_ADD8 >> MEM_MA_ADD8 R24
MEM_MA_ADD7 >> MEM_MA_ADD7 P27
MEM_MA_ADD6 >> MEM_MA_ADD6 R25
MEM_MA_ADD5 >> MEM_MA_ADD5 R26
MEM_MA_ADD4 >> MEM_MA_ADD4 R27
MEM_MA_ADD3 >> MEM_MA_ADD3 T25
MEM_MA_ADD2 >> MEM_MA_ADD2 U25
MEM_MA_ADD1 >> MEM_MA_ADD1 T27
MEM_MA_ADD0 >> MEM_MA_ADD0 W24
MEM_MA_DQS_H7 >> MEM_MA_DQS_H7 AD15
MEM_MA_DQS_L7 >> MEM_MA_DQS_L7 AE15
MEM_MA_DQS_H6 >> MEM_MA_DQS_H6 AG18
MEM_MA_DQS_L6 >> MEM_MA_DQS_L6 AG19
MEM_MA_DQS_H5 >> MEM_MA_DQS_H5 AG24
MEM_MA_DQS_L5 >> MEM_MA_DQS_L5 AG25
MEM_MA_DQS_H4 >> MEM_MA_DQS_H4 AG27
MEM_MA_DQS_L4 >> MEM_MA_DQS_L4 AG28
MEM_MA_DQS_H3 >> MEM_MA_DQS_H3 D29
MEM_MA_DQS_L3 >> MEM_MA_DQS_L3 C29
MEM_MA_DQS_H2 >> MEM_MA_DQS_H2 D25
MEM_MA_DQS_L2 >> MEM_MA_DQS_L2 C25
MEM_MA_DQS_H1 >> MEM_MA_DQS_H1 E19
MEM_MA_DQS_L1 >> MEM_MA_DQS_L1 F19
MEM_MA_DQS_H0 >> MEM_MA_DQS_H0 F15
MEM_MA_DQS_L0 >> MEM_MA_DQS_L0 G15
MEM_MA_DM7 >> MEM_MA_DM7 AF15
MEM_MA_DM6 >> MEM_MA_DM6 AF19
MEM_MA_DM5 >> MEM_MA_DM5 AJ25
MEM_MA_DM4 >> MEM_MA_DM4 AH29
MEM_MA_DM3 >> MEM_MA_DM3 B29
MEM_MA_DM2 >> MEM_MA_DM2 E18
MEM_MA_DM1 >> MEM_MA_DM1 E18
MEM_MA_DM0 >> MEM_MA_DM0 H15
MA0_CLK_H(2) MA0_CLK_L(1) MA0_CLK_H(1) MA0_CLK_L(0) MA0_CS_L(1) MA0_CS_L(0) MA0_ODT(0) MA1_CLK_H(2) MA1_CLK_L(2) MA1_CLK_H(1) MA1_CLK_L(1) MA1_CLK_H(0) MA1_CLK_L(0) MA1_CS_L(1) MA1_CS_L(0) MA1_ODT(0) MA_CAS_L MA_WE_L MA_RAS_L MA_BANK(2) MA_BANK(1) MA_BANK(0) MA_CKE(1) MA_CKE(0) MA_ADD(15) MA_ADD(14) MA_ADD(13) MA_ADD(12) MA_ADD(11) MA_ADD(10) MA_ADD(9) MA_ADD(8) MA_ADD(7) MA_ADD(6) MA_ADD(5) MA_ADD(4) MA_ADD(3) MA_ADD(2) MA_ADD(1) MA_ADD(0) MA_DQS_H(7) MA_DQS_L(7) MA_DQS_H(6) MA_DQS_L(6) MA_DQS_H(5) MA_DQS_L(5) MA_DQS_H(4) MA_DQS_L(4) MA_DQS_H(3) MA_DQS_L(3) MA_DQS_H(2) MA_DQS_L(2) MA_DQS_H(1) MA_DQS_L(1) MA_DQS_H(0) MA_DQS_L(0) MA_DM(8) MA_CHECK(7) MA_CHECK(6) MA_CHECK(5) MA_CHECK(4) MA_CHECK(3) MA_CHECK(2) MA_CHECK(1) MA_CHECK(0)

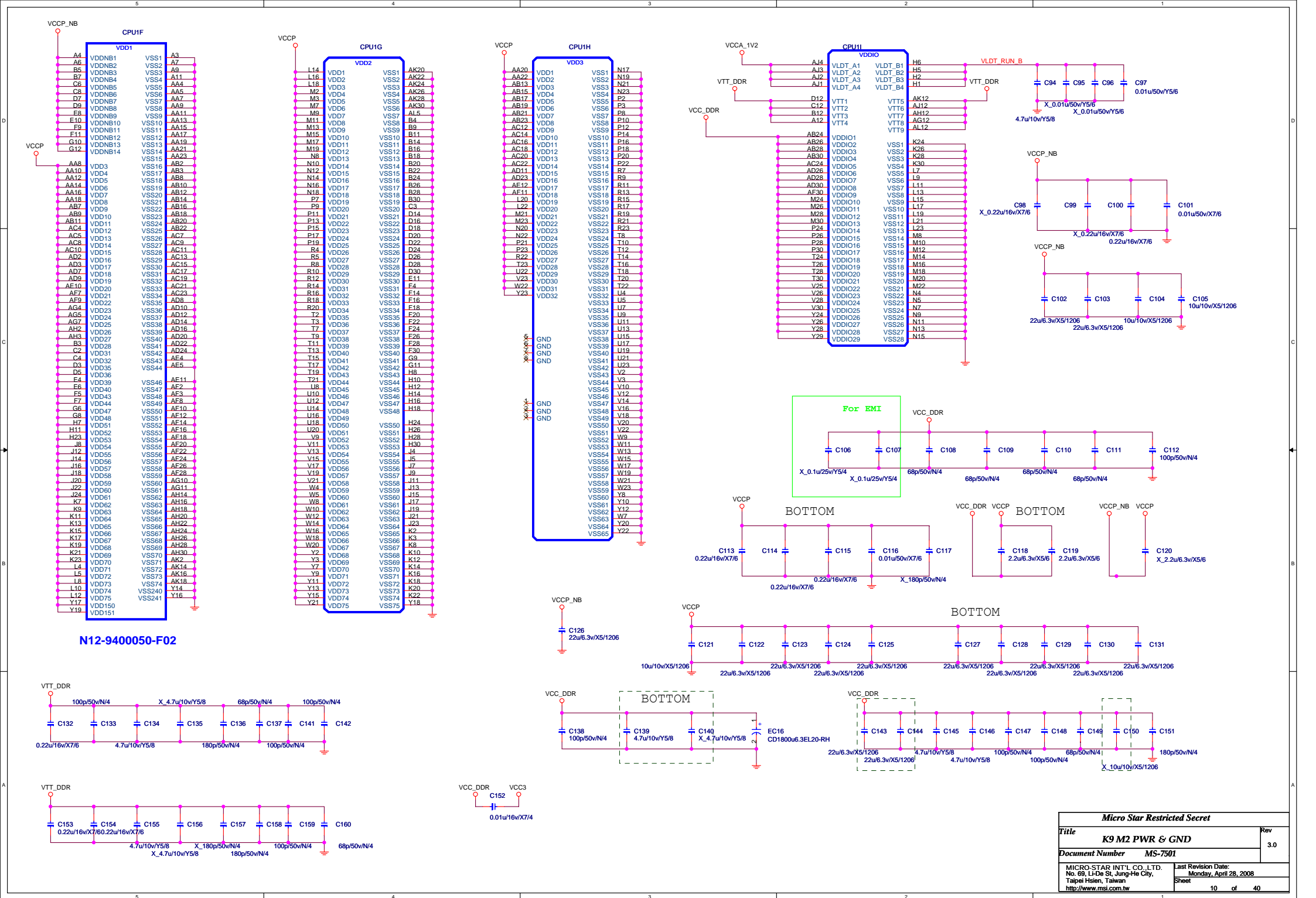
CPU1C

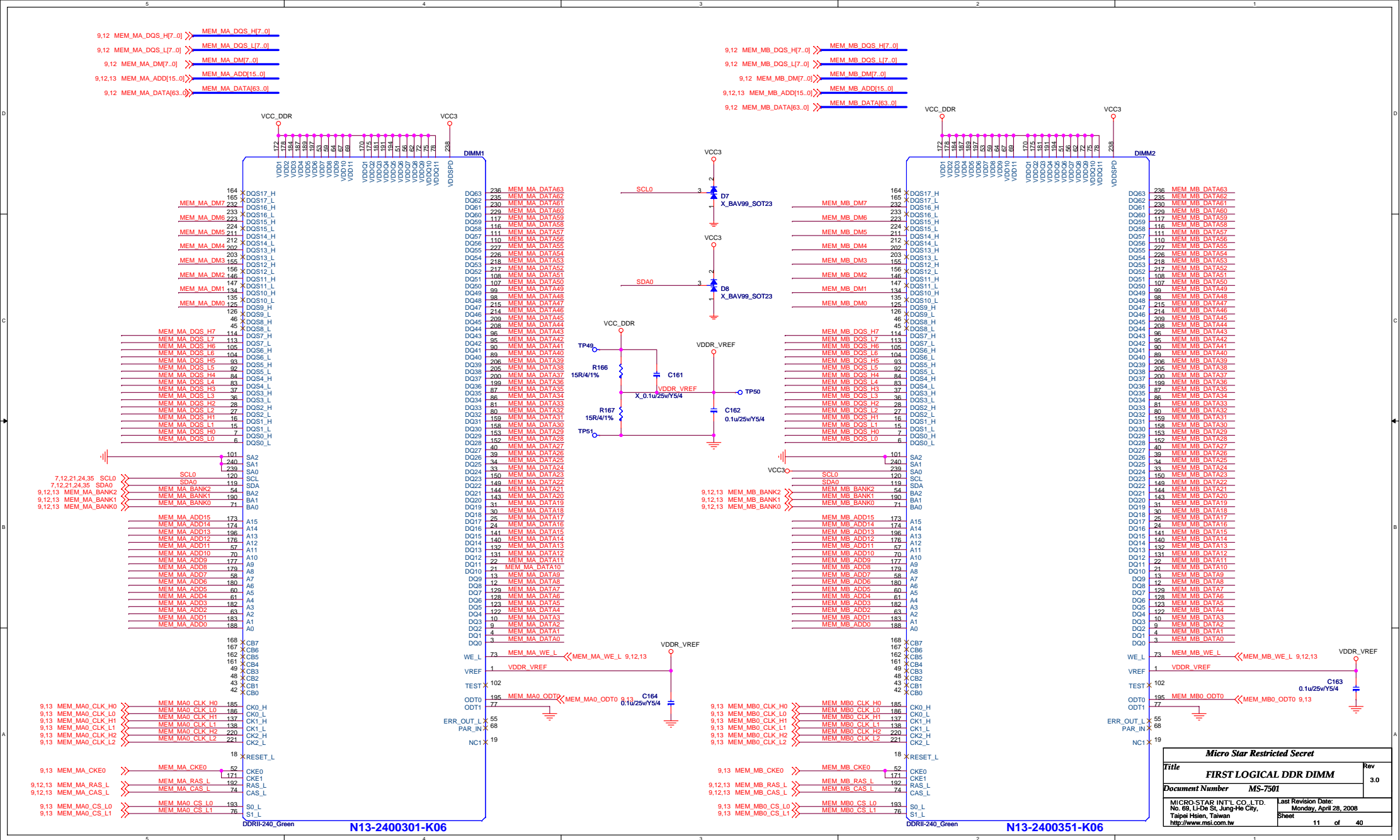
MEMORY INTERFACE B

11,13 MEM_MB0_CLK_H2 >> MEM_MB0_CLK_H2 AJ19
11,13 MEM_MB0_CLK_L2 >> MEM_MB0_CLK_L2 AK19
11,13 MEM_MB0_CLK_H1 >> MEM_MB0_CLK_H1 A18
11,13 MEM_MB0_CLK_L1 >> MEM_MB0_CLK_L1 A19
11,13 MEM_MB0_CLK_H0 >> MEM_MB0_CLK_H0 U31
11,13 MEM_MB0_CLK_L0 >> MEM_MB0_CLK_L0 U30
11,13 MEM_MB0_CS_L1 >> MEM_MB0_CS_L1 AE30
11,13 MEM_MB0_CS_L0 >> MEM_MB0_CS_L0 AC31
11,13 MEM_MB0_ODT0 >> MEM_MB0_ODT0 AD29
12,13 MEM_MB1_CLK_H2 >> MEM_MB1_CLK_H2 AL19
12,13 MEM_MB1_CLK_L2 >> MEM_MB1_CLK_L2 AL18
12,13 MEM_MB1_CLK_H1 >> MEM_MB1_CLK_H1 C19
12,13 MEM_MB1_CLK_L1 >> MEM_MB1_CLK_L1 D19
12,13 MEM_MB1_CLK_H0 >> MEM_MB1_CLK_H0 W29
12,13 MEM_MB1_CLK_L0 >> MEM_MB1_CLK_L0 W28
12,13 MEM_MB1_CS_L1 >> MEM_MB1_CS_L1 AE29
12,13 MEM_MB1_CS_L0 >> MEM_MB1_CS_L0 AB31
12,13 MEM_MB1_ODT0 >> MEM_MB1_ODT0 AD31
11,12,13 MEM_MB_CAS_L >> MEM_MB_CAS_L AC29
11,12,13 MEM_MB_WE_L >> MEM_MB_WE_L AC30
11,12,13 MEM_MB_RAS_L >> MEM_MB_RAS_L AB29
11,12,13 MEM_MB_BANK2 >> MEM_MB_BANK2 N31
11,12,13 MEM_MB_BANK1 >> MEM_MB_BANK1 AA31
11,12,13 MEM_MB_BANK0 >> MEM_MB_BANK0 AA28
12,13 MEM_MB_CKE1 >> MEM_MB_CKE1 M31
11,13 MEM_MB_CKE0 >> MEM_MB_CKE0 M29
MEM_MB_ADD15 >> MEM_MB_ADD15 N28
MEM_MB_ADD14 >> MEM_MB_ADD14 N29
MEM_MB_ADD13 >> MEM_MB_ADD13 AE31
MEM_MB_ADD12 >> MEM_MB_ADD12 N30
MEM_MB_ADD11 >> MEM_MB_ADD11 P29
MEM_MB_ADD10 >> MEM_MB_ADD10 AA29
MEM_MB_ADD9 >> MEM_MB_ADD9 P31
MEM_MB_ADD8 >> MEM_MB_ADD8 R29
MEM_MB_ADD7 >> MEM_MB_ADD7 R28
MEM_MB_ADD6 >> MEM_MB_ADD6 R31
MEM_MB_ADD5 >> MEM_MB_ADD5 R30
MEM_MB_ADD4 >> MEM_MB_ADD4 T31
MEM_MB_ADD3 >> MEM_MB_ADD3 T29
MEM_MB_ADD2 >> MEM_MB_ADD2 U29
MEM_MB_ADD1 >> MEM_MB_ADD1 U28
MEM_MB_ADD0 >> MEM_MB_ADD0 AA30
MEM_MB_DQS_H7 >> MEM_MB_DQS_H7 AK13
MEM_MB_DQS_L7 >> MEM_MB_DQS_L7 AJ13
MEM_MB_DQS_H6 >> MEM_MB_DQS_H6 AK17
MEM_MB_DQS_L6 >> MEM_MB_DQS_L6 AJ17
MEM_MB_DQS_H5 >> MEM_MB_DQS_H5 AK23
MEM_MB_DQS_L5 >> MEM_MB_DQS_L5 AL23
MEM_MB_DQS_H4 >> MEM_MB_DQS_H4 AL28
MEM_MB_DQS_L4 >> MEM_MB_DQS_L4 AL29
MEM_MB_DQS_H3 >> MEM_MB_DQS_H3 D31
MEM_MB_DQS_L3 >> MEM_MB_DQS_L3 C31
MEM_MB_DQS_H2 >> MEM_MB_DQS_H2 C24
MEM_MB_DQS_L2 >> MEM_MB_DQS_L2 C24
MEM_MB_DQS_H1 >> MEM_MB_DQS_H1 D17
MEM_MB_DQS_L1 >> MEM_MB_DQS_L1 C17
MEM_MB_DQS_H0 >> MEM_MB_DQS_H0 C14
MEM_MB_DQS_L0 >> MEM_MB_DQS_L0 C13
MEM_MB_DM7 >> MEM_MB_DM7 AJ14
MEM_MB_DM6 >> MEM_MB_DM6 AH17
MEM_MB_DM5 >> MEM_MB_DM5 AJ23
MEM_MB_DM4 >> MEM_MB_DM4 AK29
MEM_MB_DM3 >> MEM_MB_DM3 C30
MEM_MB_DM2 >> MEM_MB_DM2 B27
MEM_MB_DM1 >> MEM_MB_DM1 B17
MEM_MB_DM0 >> MEM_MB_DM0 B13
MB0_CLK_H(2) MB0_CLK_L(2) MB0_CLK_H(1) MB0_CLK_L(1) MB0_CLK_H(0) MB0_CLK_L(0) MB0_CS_L(1) MB0_CS_L(0) MB0_ODT(0) MB1_CLK_H(2) MB1_CLK_L(2) MB1_CLK_H(1) MB1_CLK_L(1) MB1_CLK_H(0) MB1_CLK_L(0) MB1_CS_L(1) MB1_CS_L(0) MB1_ODT(0) MB_CAS_L MB_WE_L MB_RAS_L MB_BANK(2) MB_BANK(1) MB_BANK(0) MB_CKE(1) MB_CKE(0) MB_ADD(15) MB_ADD(14) MB_ADD(13) MB_ADD(12) MB_ADD(11) MB_ADD(10) MB_ADD(9) MB_ADD(8) MB_ADD(7) MB_ADD(6) MB_ADD(5) MB_ADD(4) MB_ADD(3) MB_ADD(2) MB_ADD(1) MB_ADD(0) MB_DQS_H(7) MB_DQS_L(7) MB_DQS_H(6) MB_DQS_L(6) MB_DQS_H(5) MB_DQS_L(5) MB_DQS_H(4) MB_DQS_L(4) MB_DQS_H(3) MB_DQS_L(3) MB_DQS_H(2) MB_DQS_L(2) MB_DQS_H(1) MB_DQS_L(1) MB_DQS_H(0) MB_DQS_L(0) MB_DM(8) MB_CHECK(7) MB_CHECK(6) MB_CHECK(5) MB_CHECK(4) MB_CHECK(3) MB_CHECK(2) MB_CHECK(1) MB_CHECK(0)

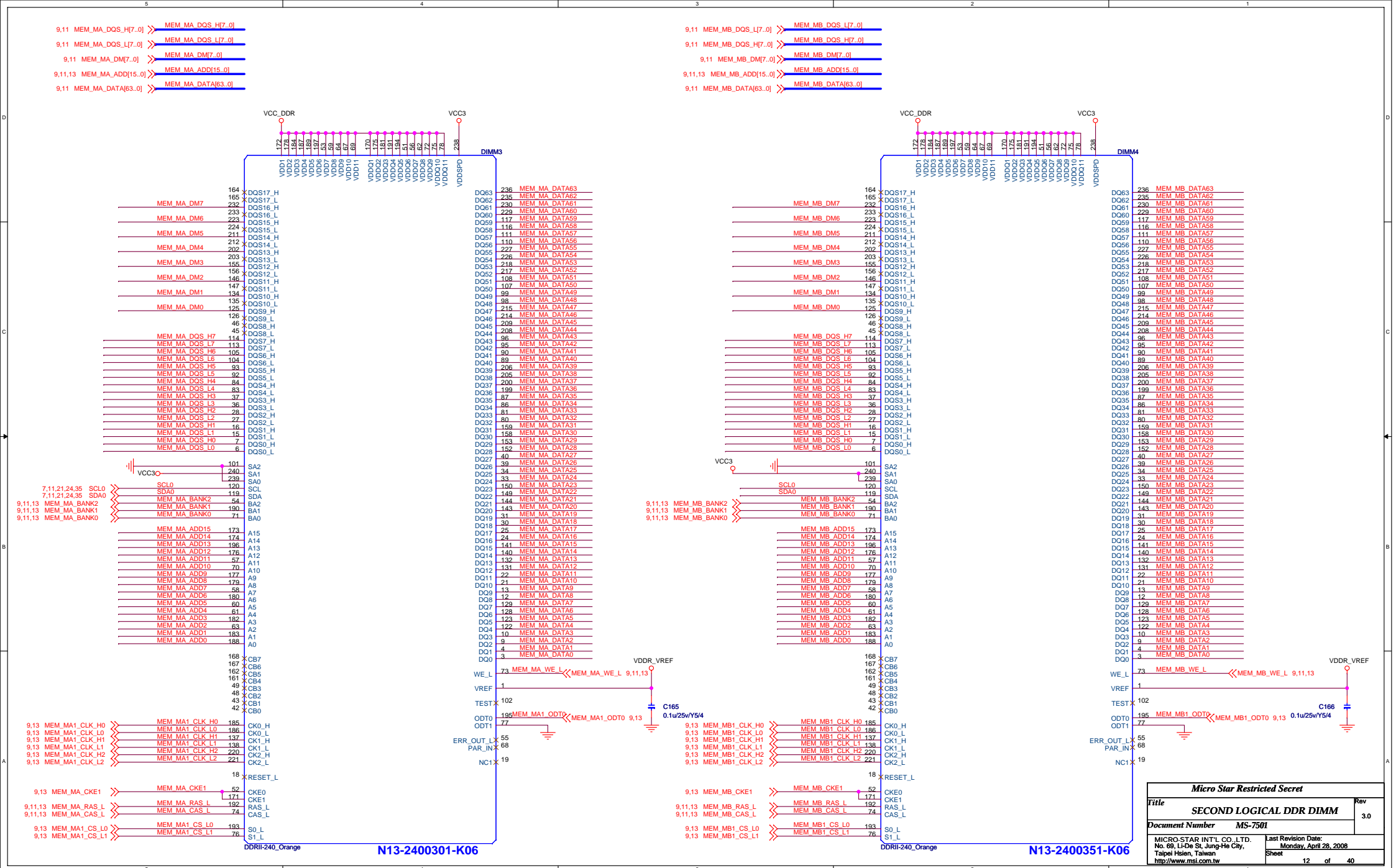
Micro Star Restricted Secret

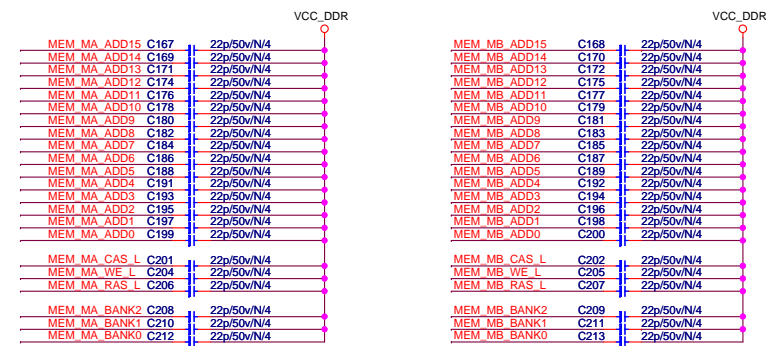
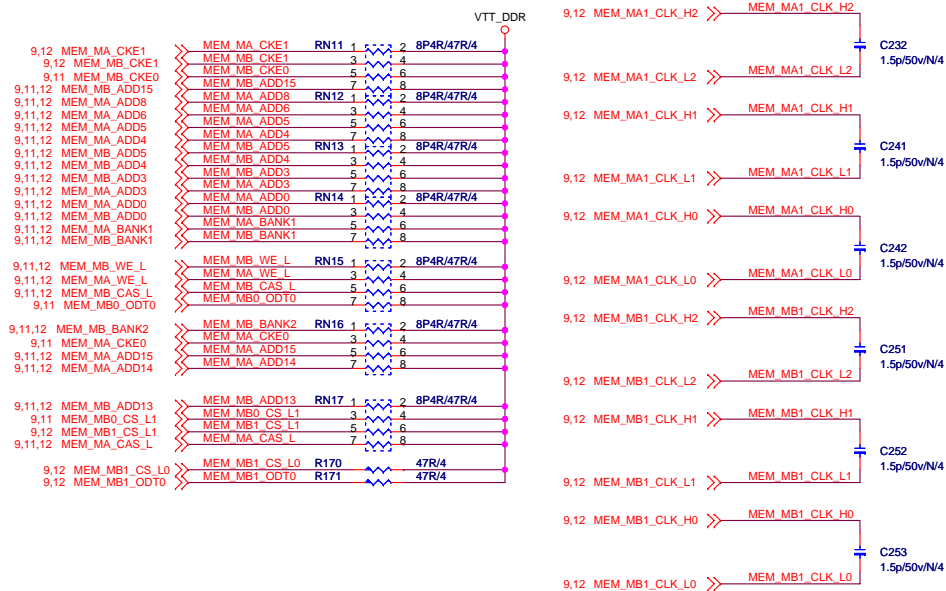
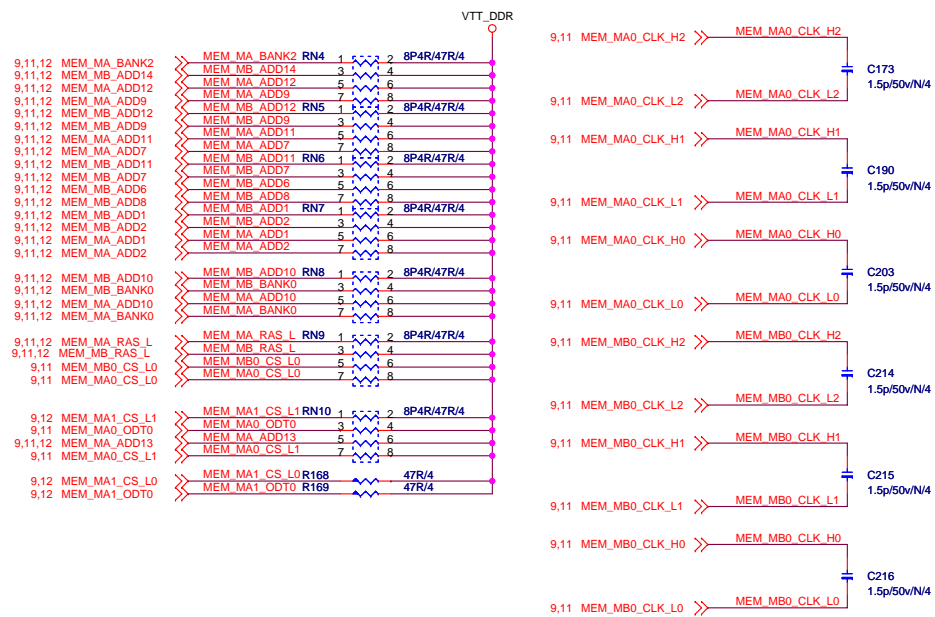
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Document Number MS-7501		
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, April 28, 2008 Sheet
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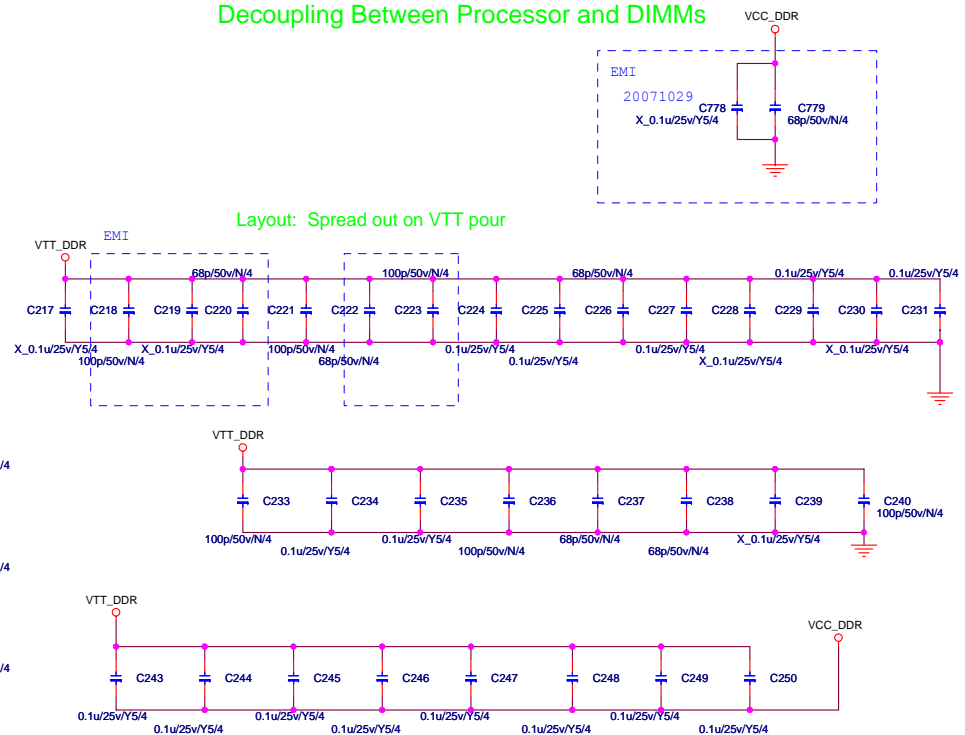


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MICRO-STAR INT'L CO., LTD. No. 69, Li-Po St, Jung-Ho City, Taippei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, April 28, 2008 Sheet 11 of 40



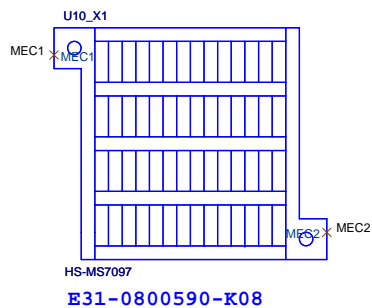


Decoupling Between Processor and DIMMs



Micro Star Restricted Secret			
Title			Rev
DDR Termination			3.0
Document Number		MS-7501	
MICRO STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, April 28, 2008 Sheet	
		13	of 40

NB HEAT-SINK



8 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
8 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]

8 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
8 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]

20 / 5 / 5 / 5 / 20

20 / 5 / 5 / 5 / 20

U10A
HT_CADOUT_H0 Y25
HT_CADOUT_L0 Y24
HT_CADOUT_H1 V22
HT_CADOUT_L1 V23
HT_CADOUT_H2 V25
HT_CADOUT_L2 V24
HT_CADOUT_H3 U24
HT_CADOUT_L3 U25
HT_CADOUT_H4 T25
HT_CADOUT_L4 T24
HT_CADOUT_H5 P23
HT_CADOUT_L5 P22
HT_CADOUT_H6 P25
HT_CADOUT_L6 P24
HT_CADOUT_H7 N24
HT_CADOUT_L7 N25
HT_CADOUT_H8 AC24
HT_CADOUT_L8 AC25
HT_CADOUT_H9 AB25
HT_CADOUT_L9 AB24
HT_CADOUT_H10 AA24
HT_CADOUT_L10 AA25
HT_CADOUT_H11 Y22
HT_CADOUT_L11 Y23
HT_CADOUT_H12 W21
HT_CADOUT_L12 W20
HT_CADOUT_H13 V21
HT_CADOUT_L13 V20
HT_CADOUT_H14 U20
HT_CADOUT_L14 U21
HT_CADOUT_H15 U19
HT_CADOUT_L15 U18

PART 1 OF 6

HYPER TRANSPORT CPU
I/F

HT_TXCAD0P D24
HT_TXCAD0N D25
HT_TXCAD1P E24
HT_TXCAD1N E25
HT_TXCAD2P F24
HT_TXCAD2N F25
HT_TXCAD3P F22
HT_TXCAD3N F23
HT_TXCAD4P H23
HT_TXCAD4N H22
HT_TXCAD5P J25
HT_TXCAD5N J24
HT_TXCAD6P K24
HT_TXCAD6N K25
HT_TXCAD7P K23
HT_TXCAD7N K22
HT_TXCAD8P G21
HT_TXCAD8N G20
HT_TXCAD9P H21
HT_TXCAD9N H20
HT_TXCAD10P J21
HT_TXCAD10N J18
HT_TXCAD11P K17
HT_TXCAD11N K19
HT_TXCAD12P L19
HT_TXCAD12N L18
HT_TXCAD13P M19
HT_TXCAD13N M18
HT_TXCAD14P M21
HT_TXCAD14N M20
HT_TXCAD15P P18
HT_TXCAD15N P17

8 HT_CLKOUT_H0 >>>
8 HT_CLKOUT_L0 >>>
8 HT_CLKOUT_H1 >>>
8 HT_CLKOUT_L1 >>>
8 HT_CTLOUT_H0 >>>
8 HT_CTLOUT_L0 >>>
8 HT_CTLOUT_H1 >>>
8 HT_CTLOUT_L1 >>>

T22 HT_RXCLK0P
AB23 HT_RXCLK0N
AA22 HT_RXCLK1P
HT_RXCLK1N
M22 HT_RXCTL0P
M23 HT_RXCTL0N
R21 HT_RXCTL1P
R20 HT_RXCTL1N

301R/4/1% R172 HT_RXCALP
HT_RXCALN A24

5 / 10

H24 HT_TXCLK0P
H25 HT_TXCLK0N
L21 HT_TXCLK1P
L20 HT_TXCLK1N
M24 HT_TXCTL0P
M25 HT_TXCTL0N
P19 HT_TXCTL1P
R18 HT_TXCTL1N

8 HT_CLKIN_H0 >>>
8 HT_CLKIN_L0 >>>
8 HT_CLKIN_H1 >>>
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8 HT_CTLIN_L0 >>>
8 HT_CTLIN_H1 >>>
8 HT_CTLIN_L1 >>>

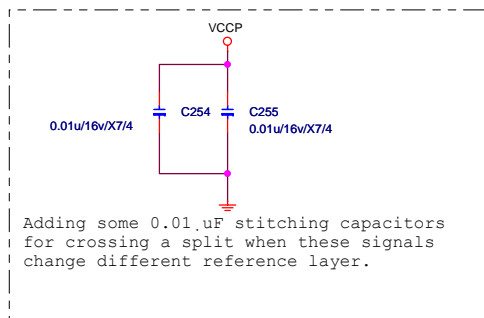
B24 HT_TXCALP
B25 HT_TXCALN

5 / 10

Check U10 New Version : Port Number

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)	1.21K	301R
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



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Title			RS780-HT L
Size	Document Number	MS-7501	
Date:	Monday, April 28, 2008	Sheet	14 of 40
			Rev 3.0

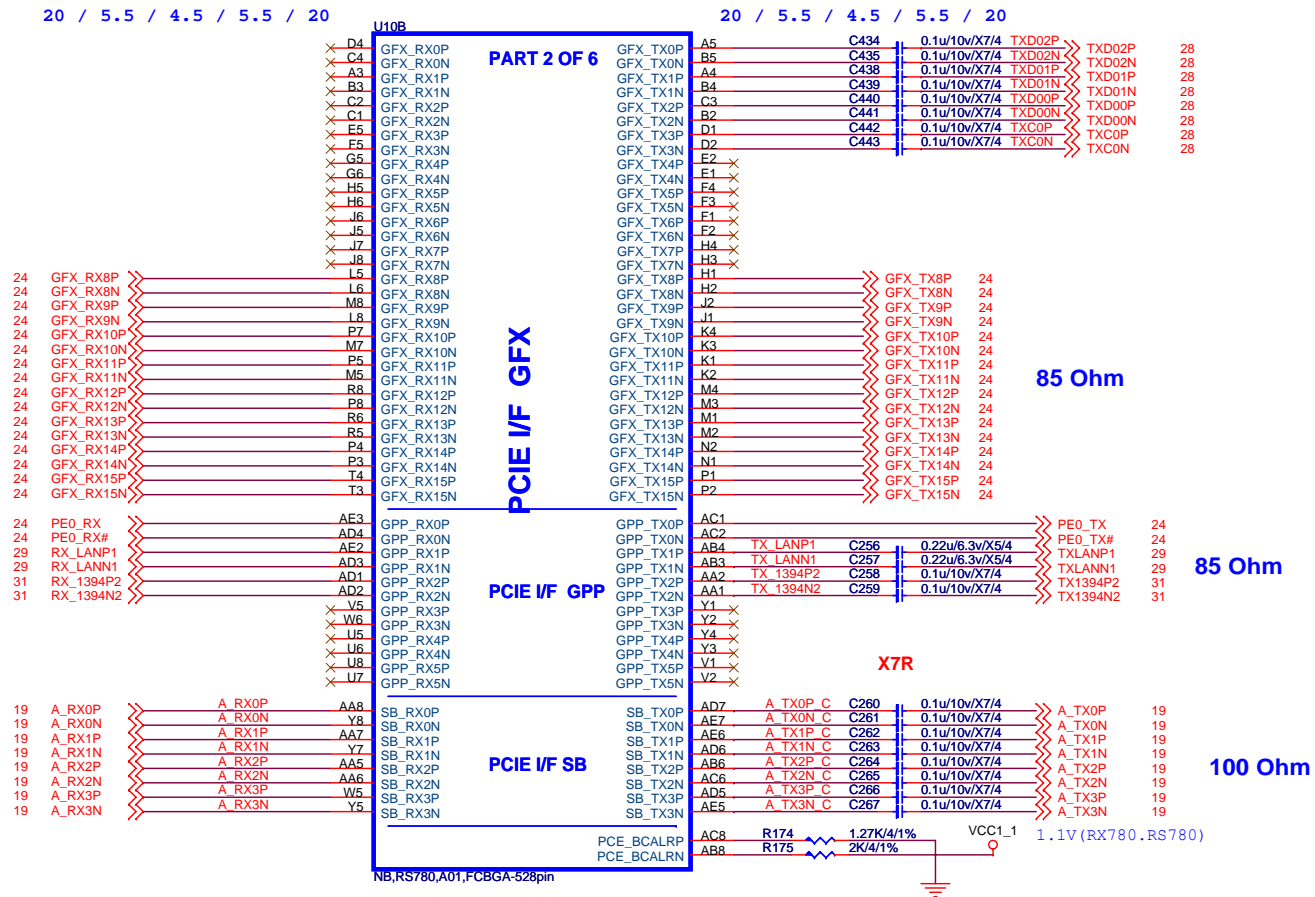
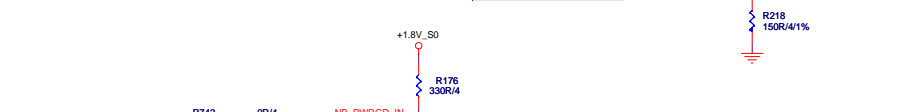
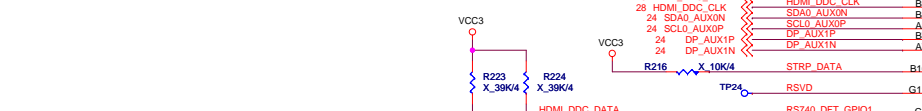
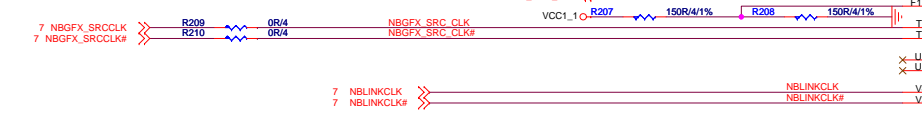
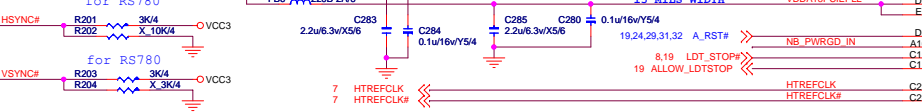
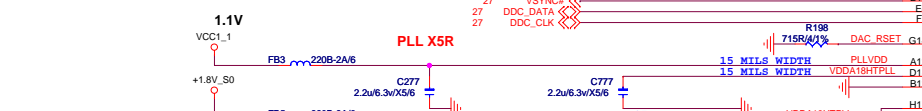
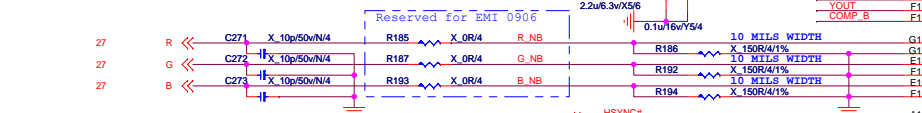
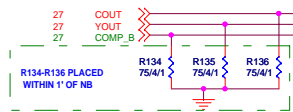


Figure 39: Layout Guidelines for the PCI-Express Expansion Interface



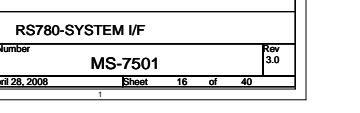
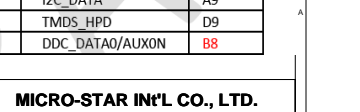
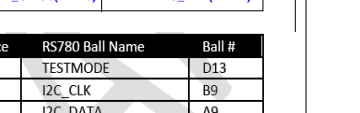
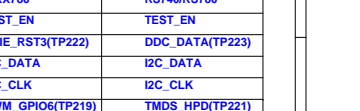
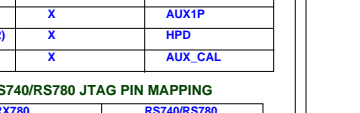
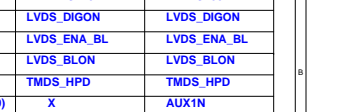
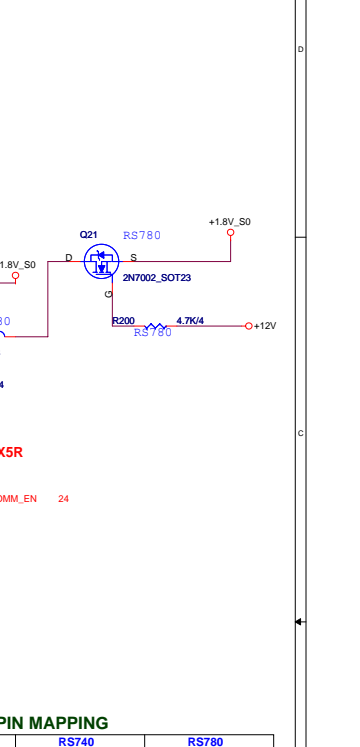
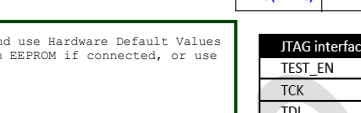
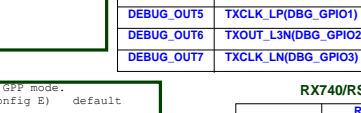
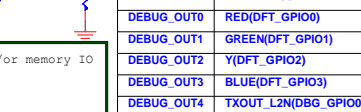
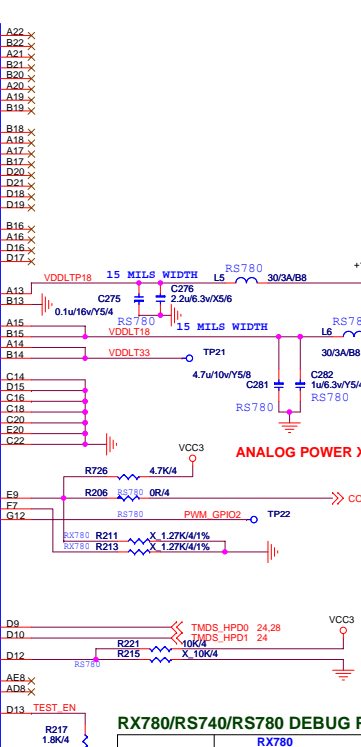
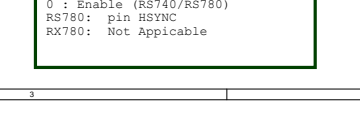
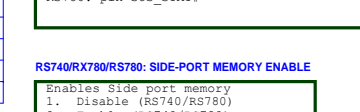
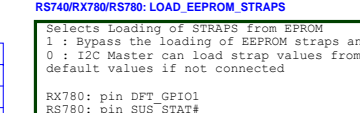
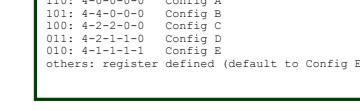
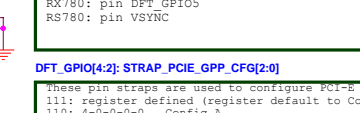
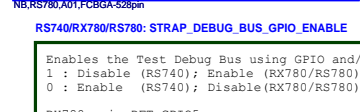
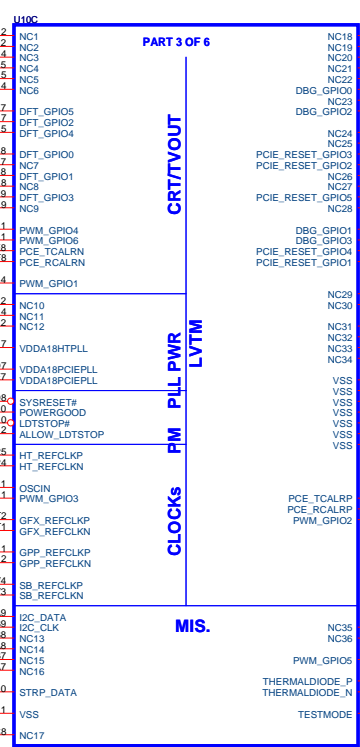
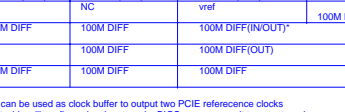
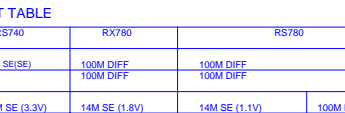
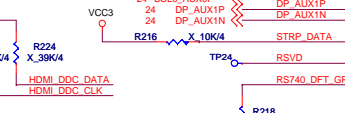
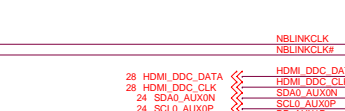
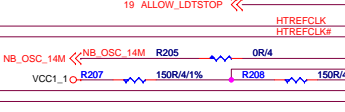
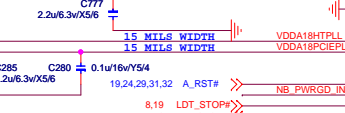
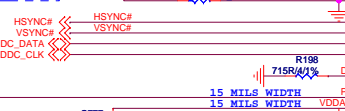
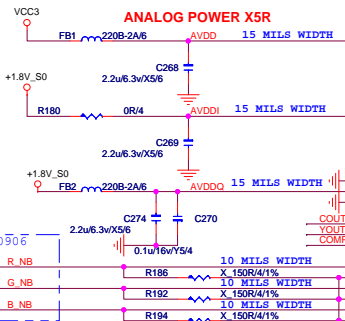
RX740/RX740/RX780 difference table			
	RS740	RX780	RS780
NB_PWRGD_IN	3.3V IN	1.8V IN	1.8V IN
ALLOW_LDTSTOP_OUT(default)/IN	OC	OC	OC/3.3V IN
LDT_STOP#IN(default)/IN	3.3V IN	1.8V IN	3.3V IN/OC

* CLMC mode: NB send LDT_STOP#, ALLOW_LDTSTOP will become input

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GPX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIe reference clocks
By default, chip will configured as input mode, BIOS can program it to output mode.



RX780/RS740/RS780 DEBUG PIN MAPPING

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPIO0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPIO1)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPIO2)	LVDS_BLON	LVDS_BLON
DEBUG_OUT3	BLUE(DFT_GPIO3)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPIO0)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPIO1)	X	HPD
DEBUG_OUT6	TXOUT_L3N(DBG_GPIO2)	X	AUX_CAL
DEBUG_OUT7	TXCLK_LN(DBG_GPIO3)	X	

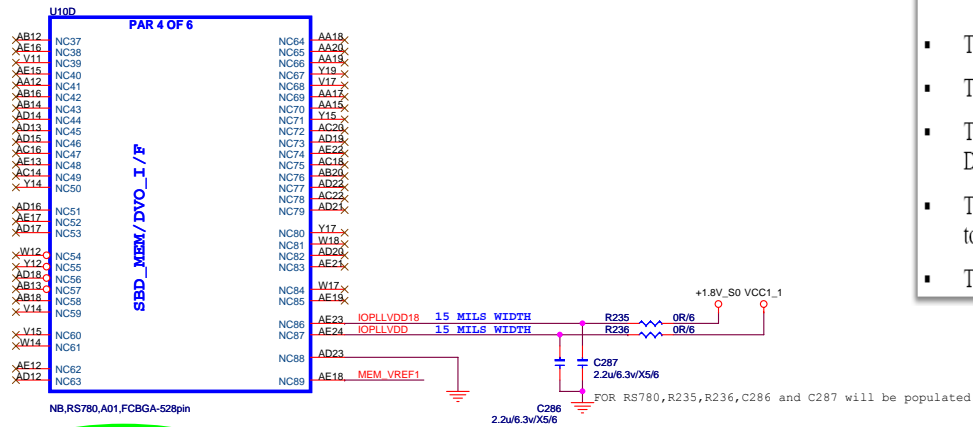
RX740/RS740/RS780 JTAG PIN MAPPING

	RX780	RS740/RS780
TRST	TEST_EN	TEST_EN
TMS(TP220)	PCIE_RST3(TP222)	DDC_DATA(TP223)
TDI	I2C_DATA	I2C_DATA
TCK	I2C_CLK	I2C_CLK
TDO(TP218)	PWM_GPIO6(TP219)	TMDS_HPD(TP221)

JTAG interface	RS780 Ball Name	Ball #
TEST_EN	TESTMODE	D13
TCK	I2C_CLK	B9
TDI	I2C_DATA	A9
TDO	TMDS_HPD	D9
TMS	DDC_DATA/AUXON	B8

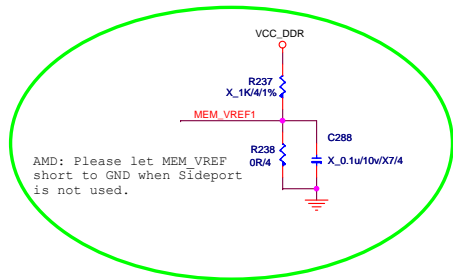
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RS780-SYSTEM I/F		
File	Document Number	Rev 3.0
MS-7501		
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Note: If the Side-port memory interface is **not** used, make sure that:

- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVDD18 is connected to 1.8 V and IOPLLVDD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.



Max Power Estimates for RS780 and SB700

(Preliminary Data w/ Internal Clock Generator and IMC disabled)

April 2007

Voltage	Usage	Domain	Max(Spec)
1.0-1.1V	RS780	S0/S1	10A
1.1V	RS780	S0/S1	3-4A
1.2V	RS780 & SB700	S0/S1	2.4A (1A-NB / 1.4A-SB)
1.8V	RS780& SB700	S0/S1	0.8A (0.75A-NB / 50mA-SB)

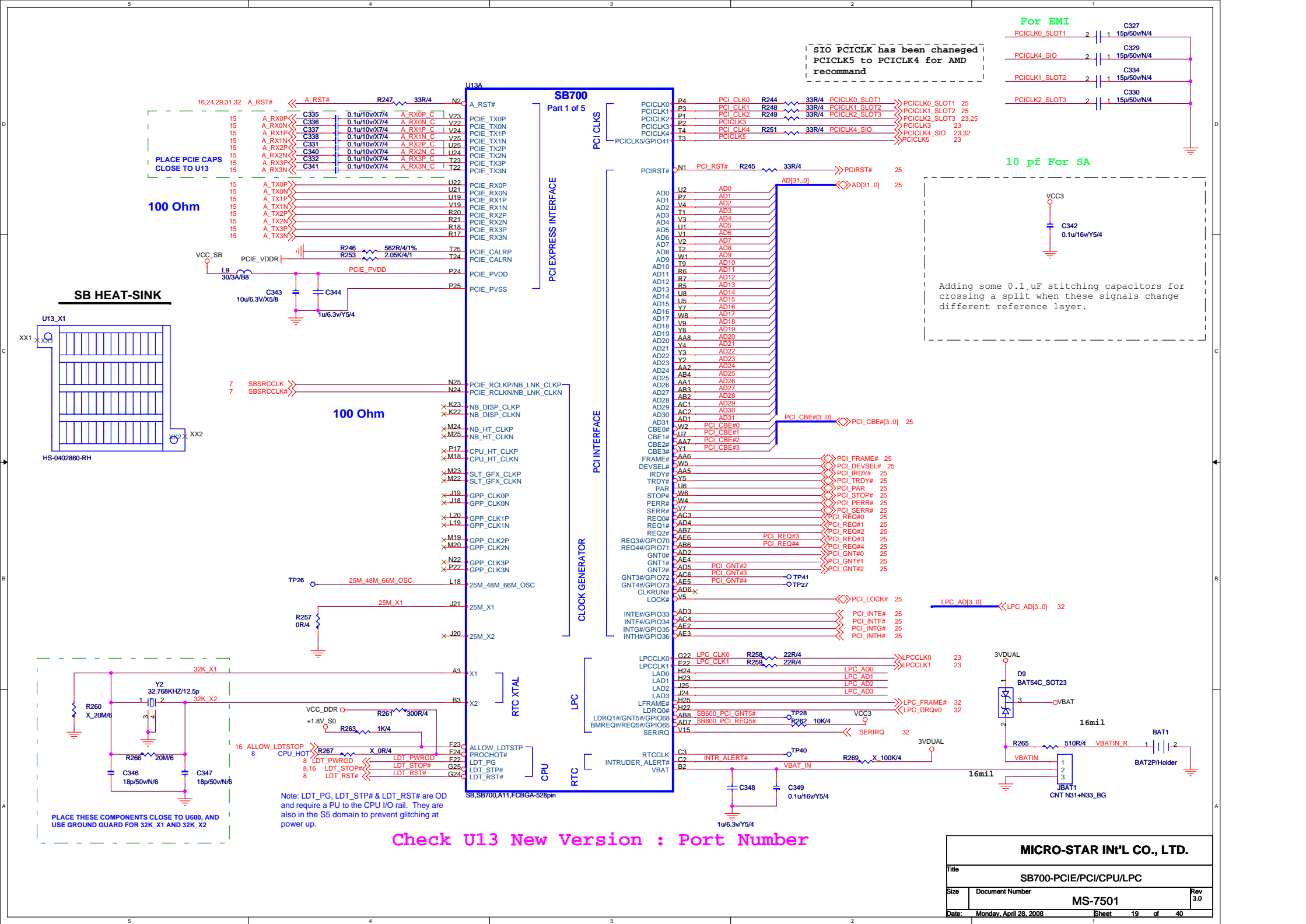
Max Power Estimates for RS780 and SB700 (continued)

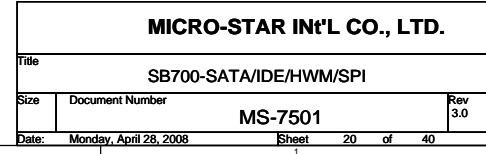
April 2007

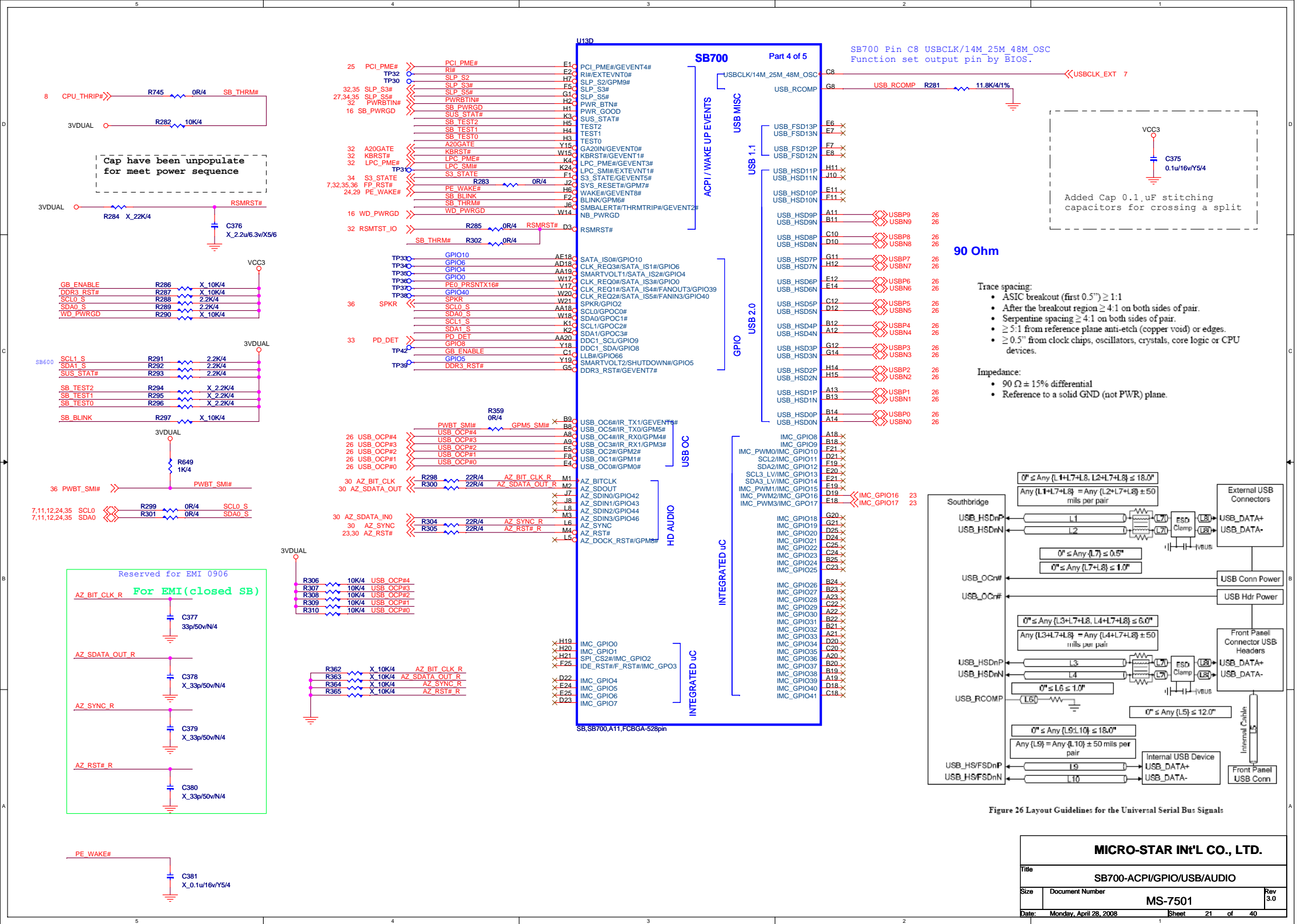
Voltage	Usage	Domain	Max(Spec)
3.3V	RS780& SB700	S0/S1	428mA (0.3A-NB / 128mA-SB)
1.2VDual	SB700	S0/S1/S2/S3/S4/S5	217mA
3.3VDual	SB700	S0/S1/S2/S3/S4/S5	495mA
5V	SB700 V5_VREF	S0/S1	0.21mA

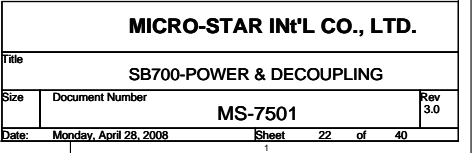
MICRO-STAR INT'L CO., LTD.

File		RS780-SPMEM/STRAPS	
Size	Document Number	MS-7501	Rev 3.0
Date	Monday, April 28, 2008	Sheet 17 of 40	





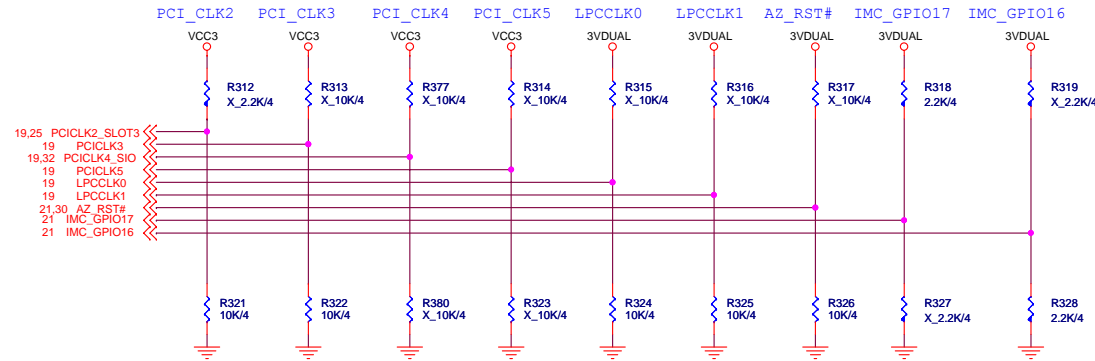






REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	IMC DISABLED DEFAULT	L, H = LPC ROM L, L = FWH ROM DEFAULT	

DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

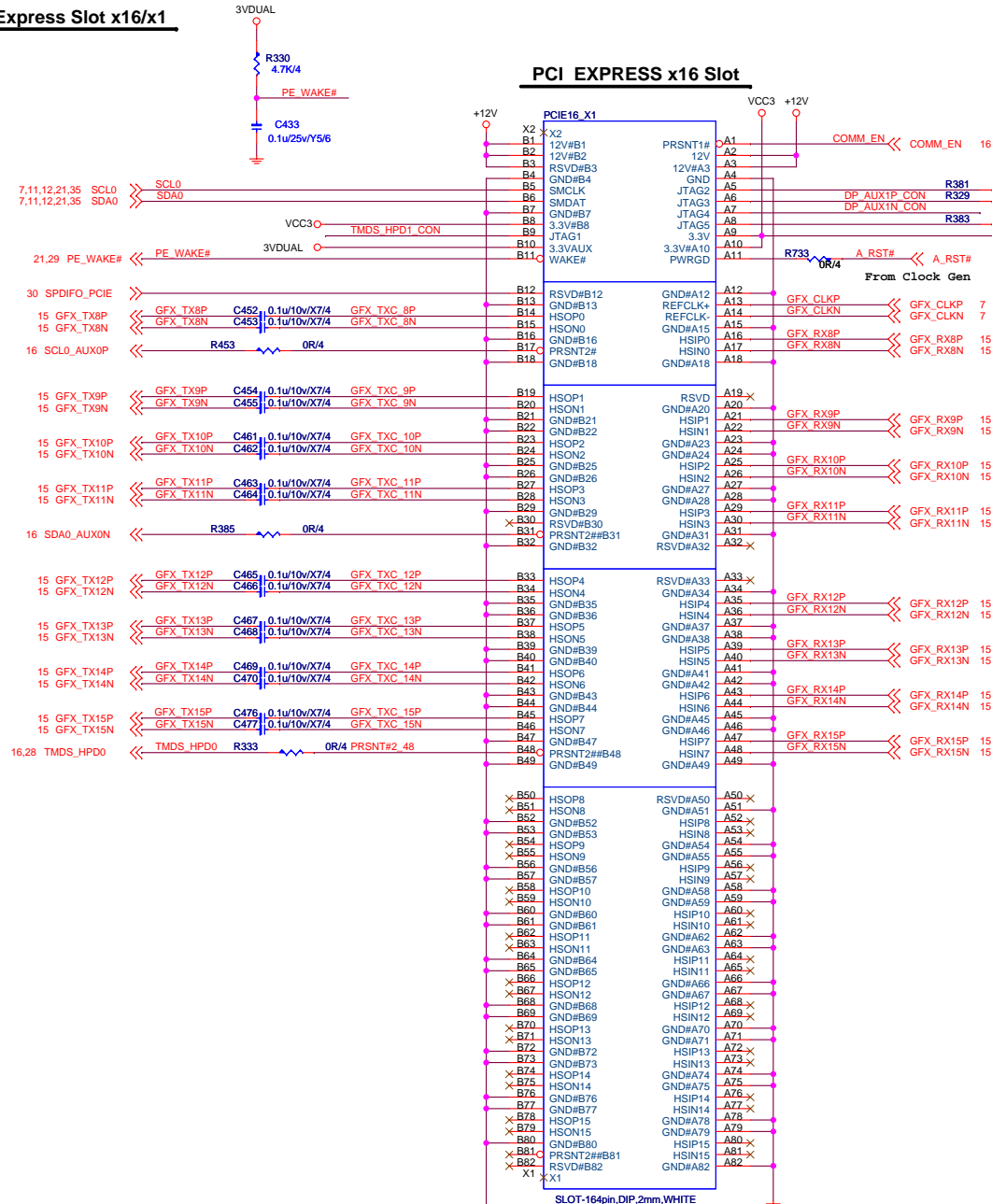
MICRO-STAR INT'L CO., LTD.

Title				SB700-STRAPS			
Size	Document Number			MS-7501			Rev 3.0
Date:	Monday, April 28, 2008			Sheet	23	of	40

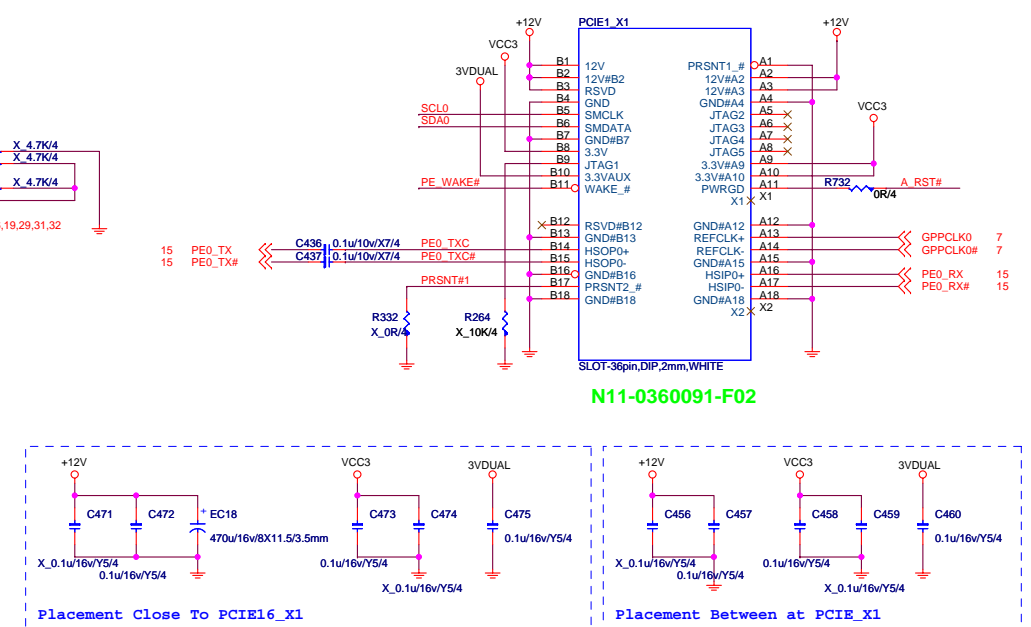
PCI Express Slot x16/x1

PCI EXPRESS 1 Slot-1

PCI EXPRESS x16 Slot

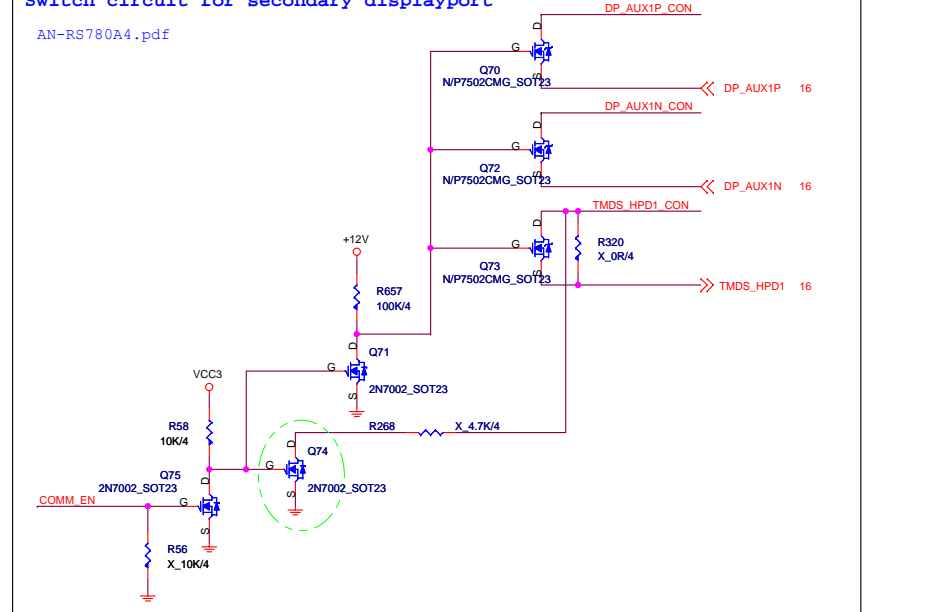


N11-1640401-K06



Switch circuit for secondary displayport

AN-RS780A4.pdf



MSI
Link to the Future
MICRO-START INT'L CO.,LTD.

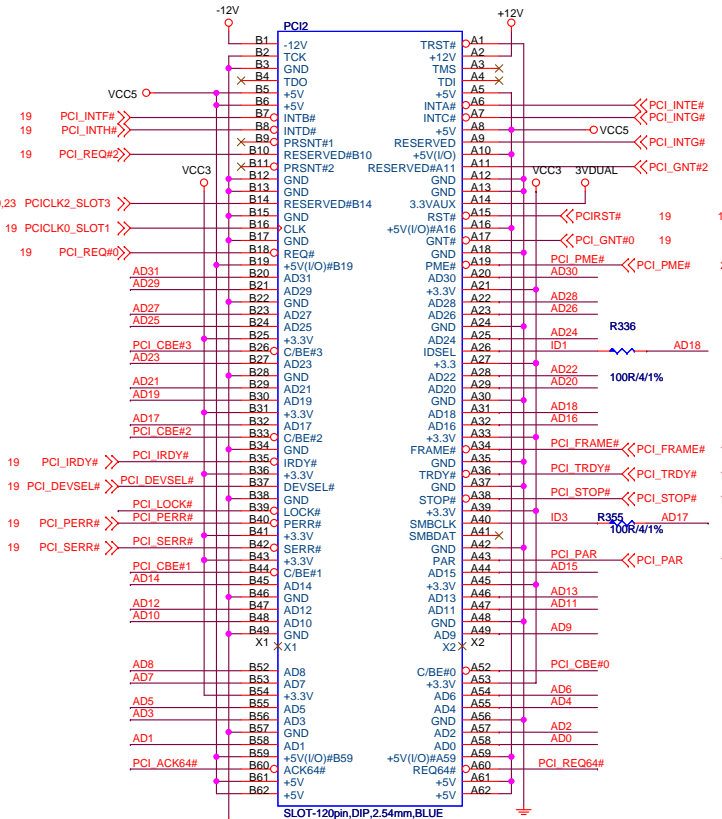
PCI EXPRESS X16 & X1 SLOT

Size Custom Document Number MS-7501 Rev 3.0

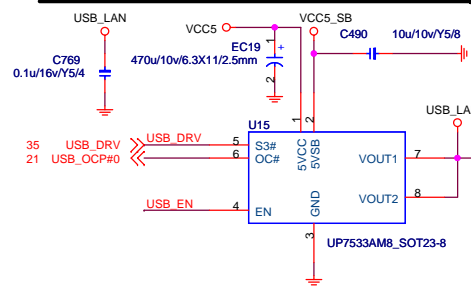
Date: Monday, April 28, 2008 Sheet 24 of 40

19 AD[31..0] >> AD[31..0]
19 PCI_CBE#[3..0] >> PCI_CBE#[3..0]

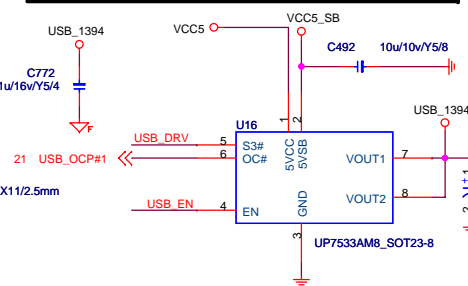
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



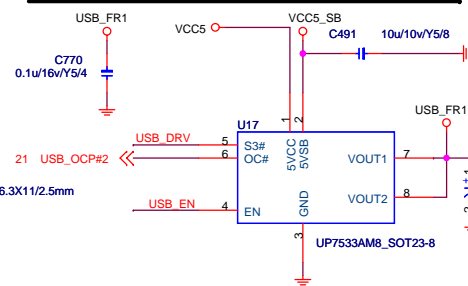
POWER CIRCUIT FOR USB PORT 4,5



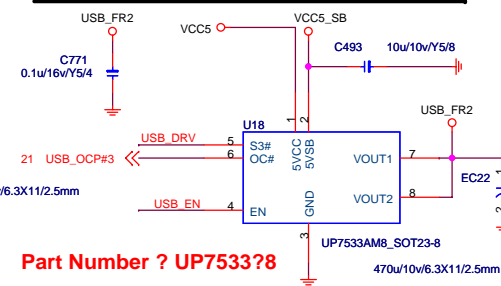
POWER CIRCUIT FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1



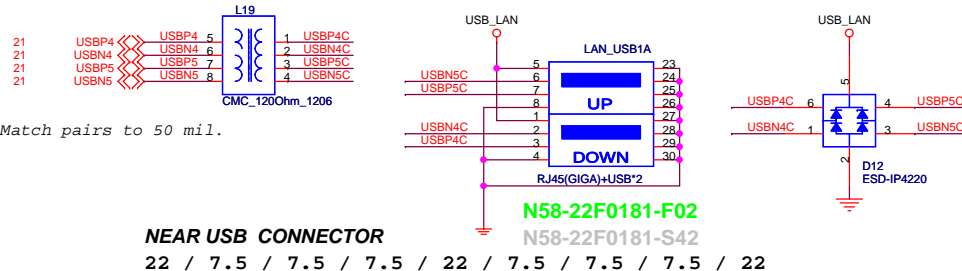
POWER CIRCUIT FOR USB PORT 6,7



Part Number ? UP7533?8

REAR PANEL USB CONNECTOR FOR USB PORT 4,5

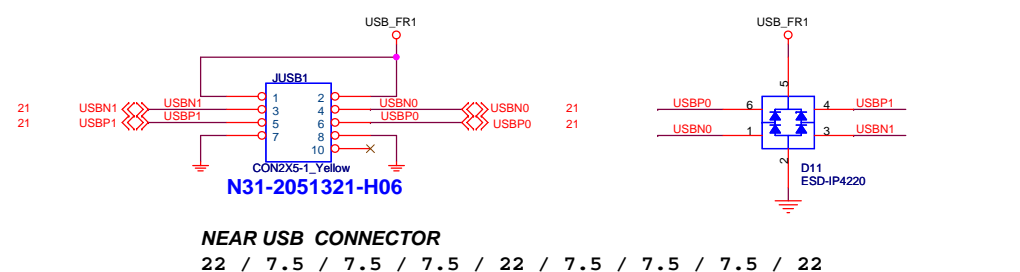
Trace lengths must be less 12 inches



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 0,1

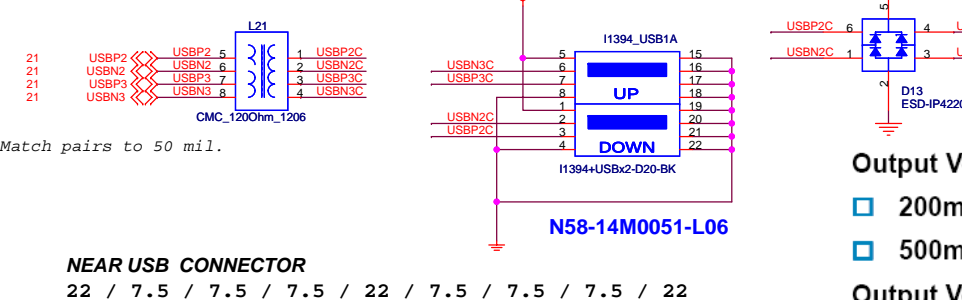


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

REAR PANEL USB CONNECTOR FOR USB PORT 2,3

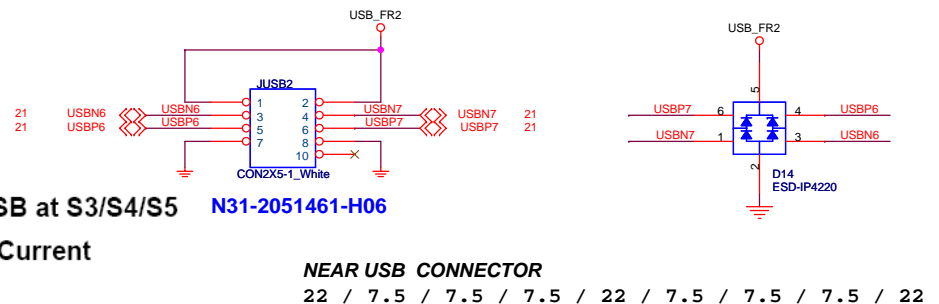
Trace lengths must be less 12 inches



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

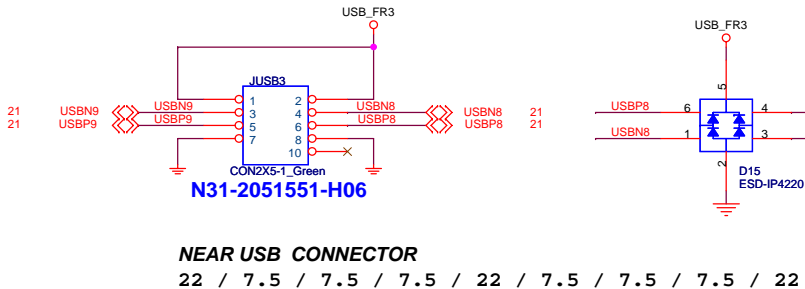


NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

Trace lengths must be less 5 inches



NEAR USB CONNECTOR

22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

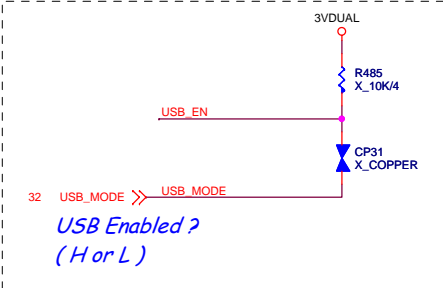
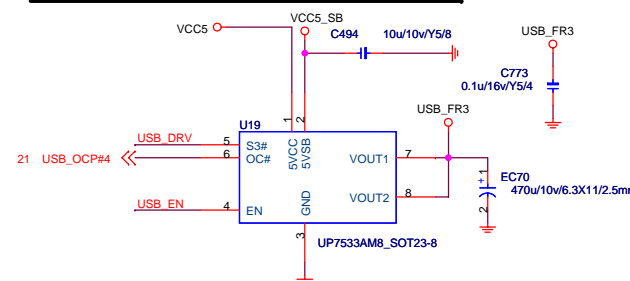
Output Voltage Switch to 5VSB at S3/S4/S5

- 200mA Continuous Load Current
- 500mΩ High Side Switch

Output Voltage Switch to 5VCC at S0/S1/S2

- 1.5A Continuous Load Current
- 110mΩ High Side Switch

POWER CIRCUIT FOR USB PORT 8,9

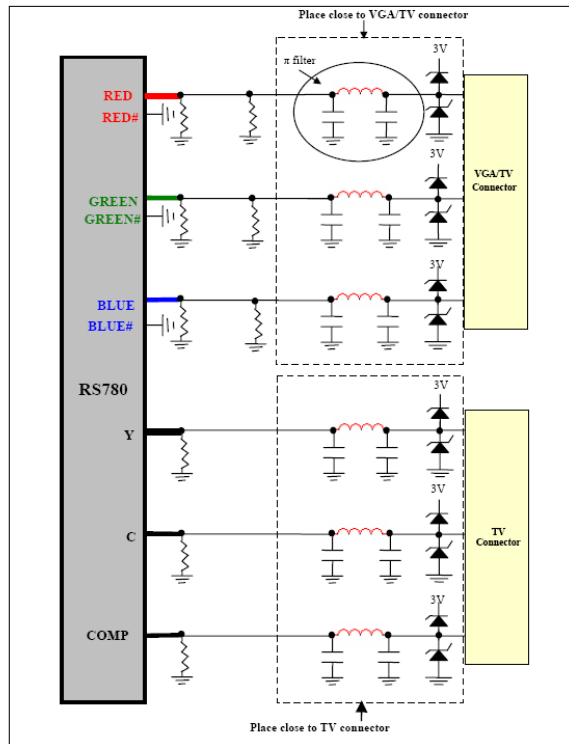


USB Enabled ?
(H or L)

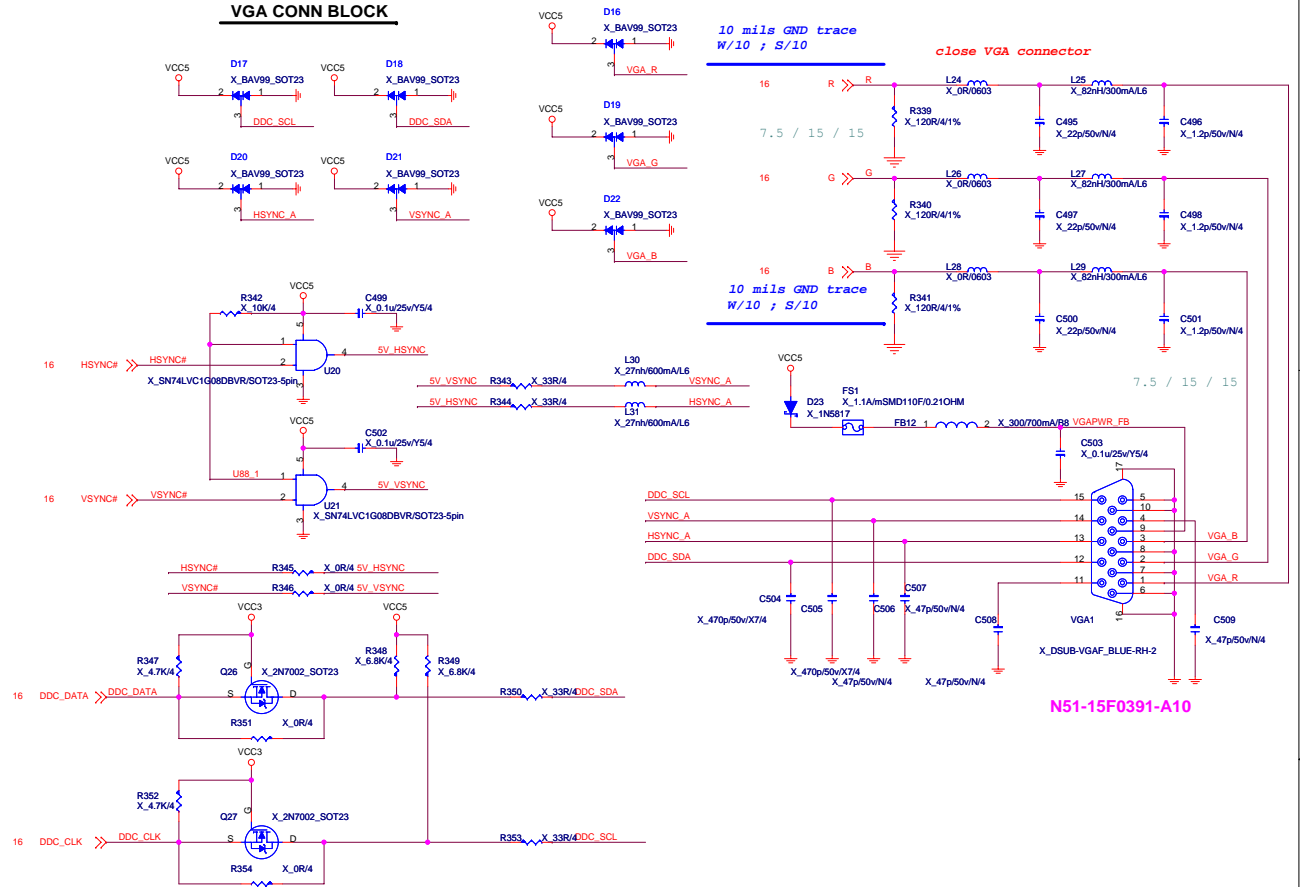
MICRO-STAR IN'L CO., LTD.

Title			USB Conn.
Size	Document Number	MS-7501	
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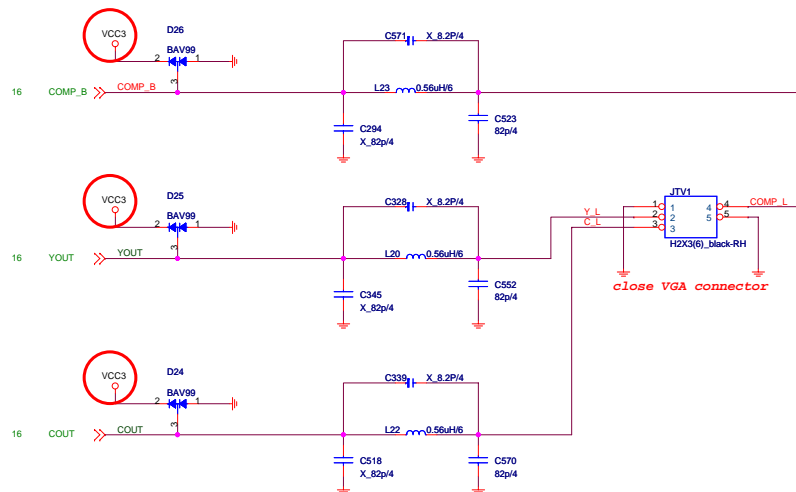
Figure 29: Placement of VGA and TV-Out Connectors



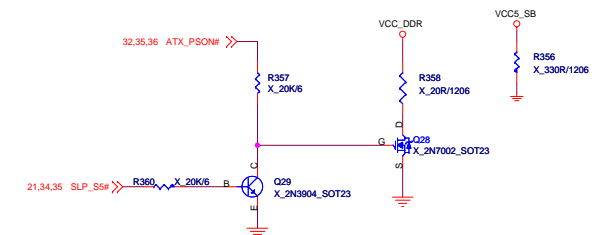
VGA CONN BLOCK



TV_OUT CONNECTOR



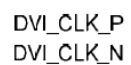
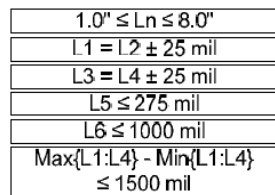
MEMORY VOLTAGE BLEED-OFF CIRCUIT



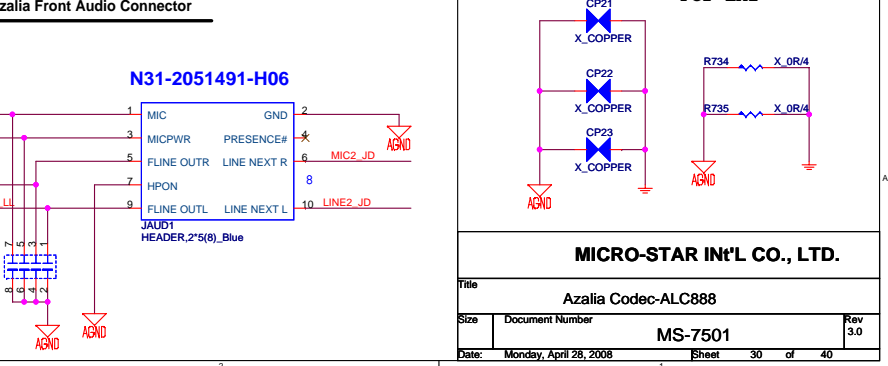
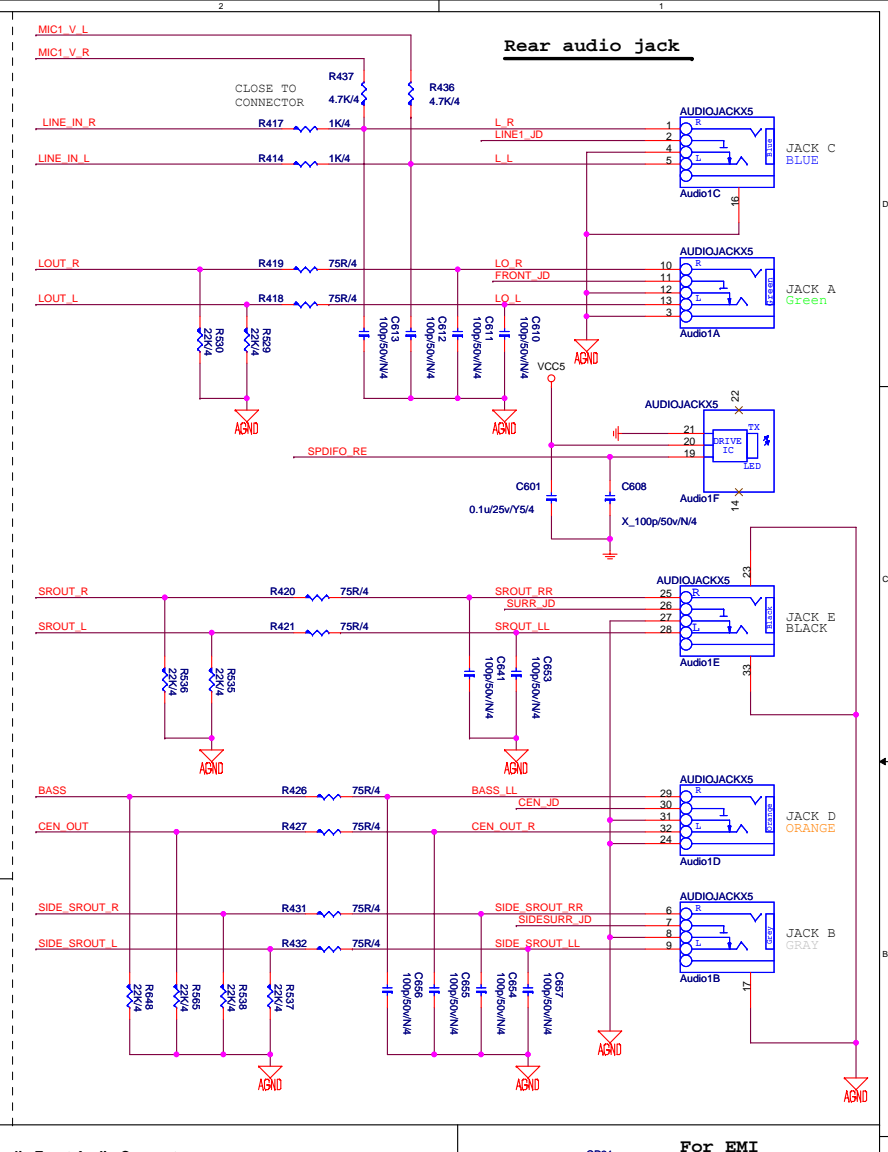
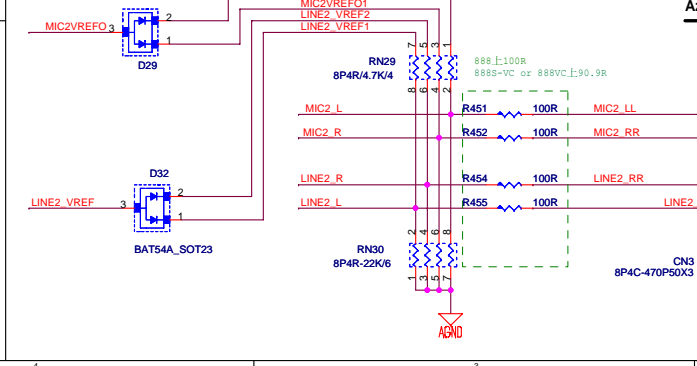
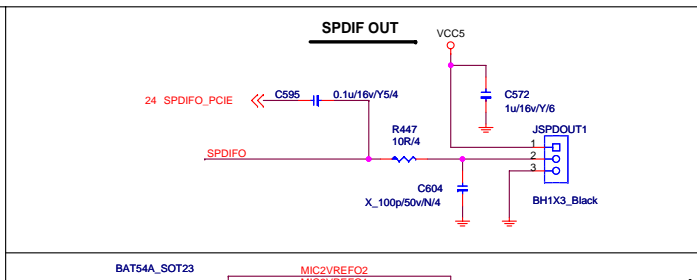
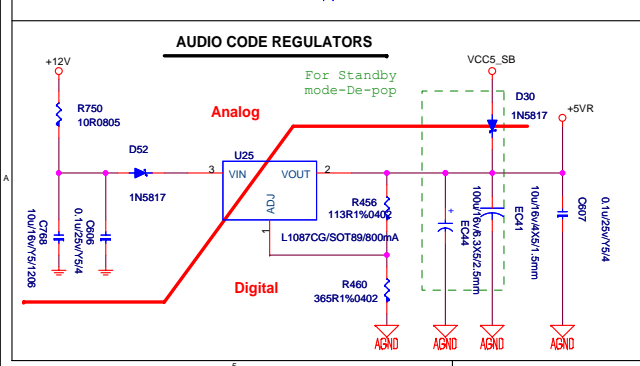
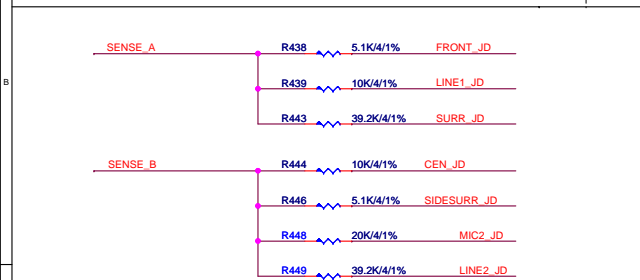
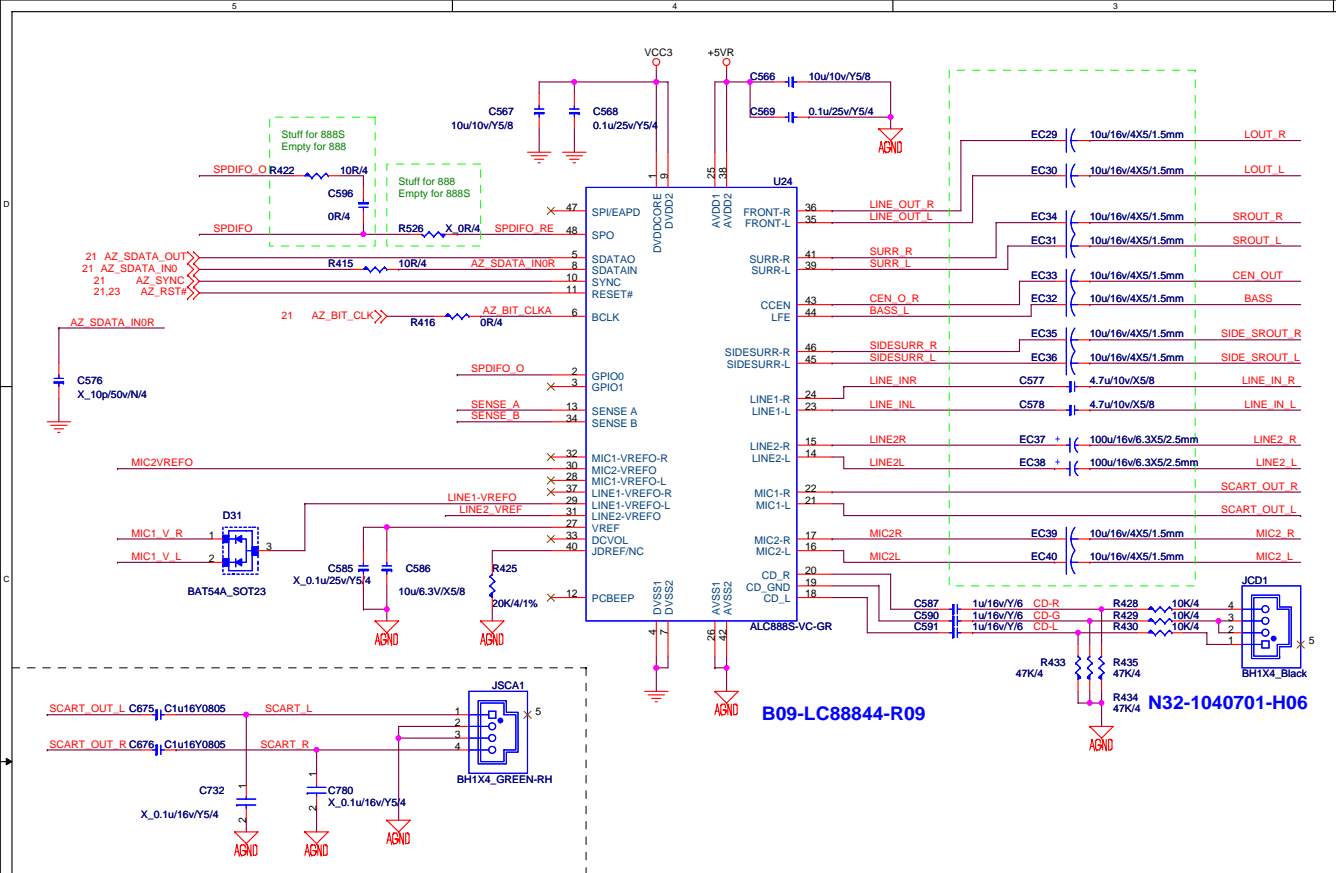
MICRO-STAR INT'L CO., LTD.

File	VGA CONN		
Size	Document Number	MS-7501	Rev 3.0
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15 / 5 / 7 / 5 / 15



Title			
HDMI CONNECTOR			
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1394 CONTROLLER

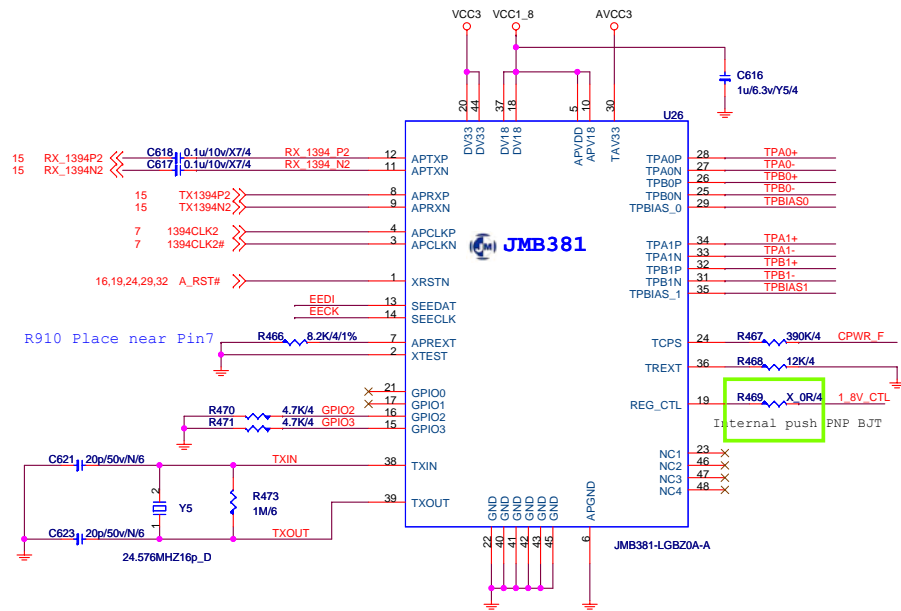
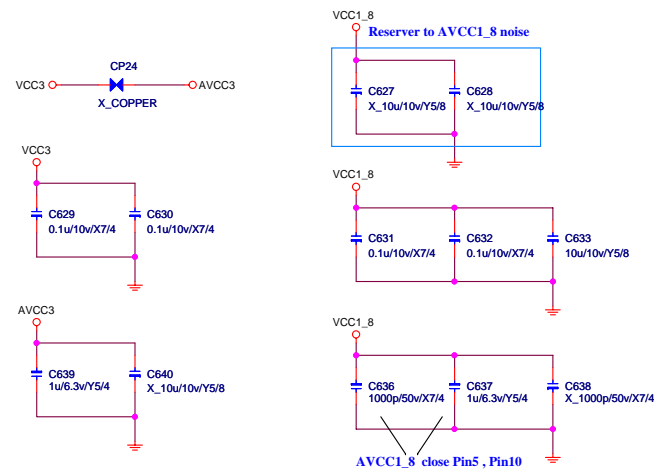
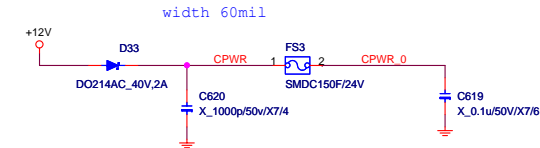
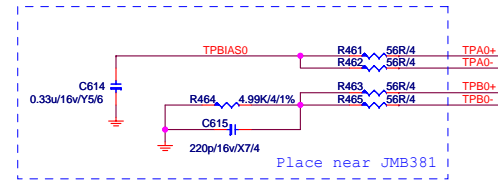


Table 5.1 JMB381 Operating Modes

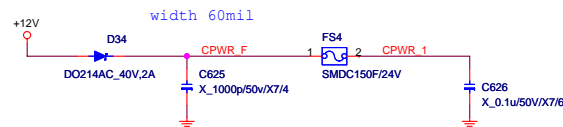
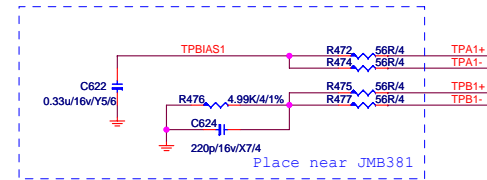
	Normal	IDDQ	BIST/FL	Nandtree
XTEST	0	1	1	1
GPIO2	x	0	0	1
GPIO3	x	0	1	1



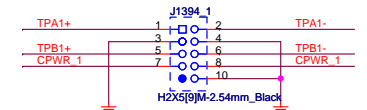
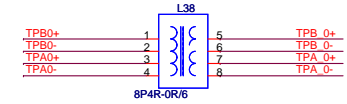
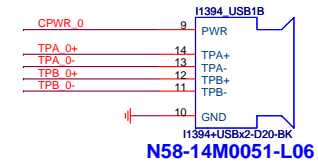
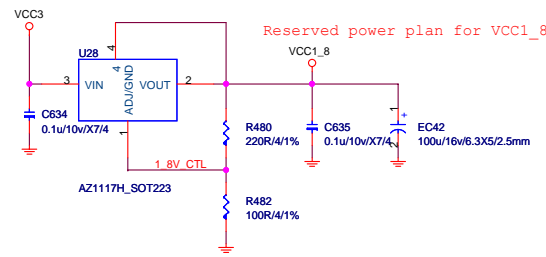
Rear 1394 port



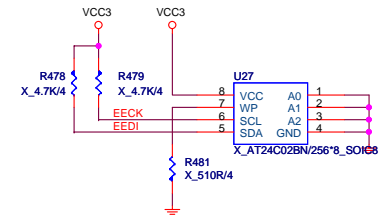
Front 1394 pin header



A1117 CO-LAY SOT223 (TO_261) PNP BJT




For Intel 1394 pinheader



S3 Resume time

Title			
1394 Controller - JMB381			
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 MICRO-STAR INT'L CO., LTD.	
Title	
LPC-F71882 / FDD / VFD	
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	MS-7501
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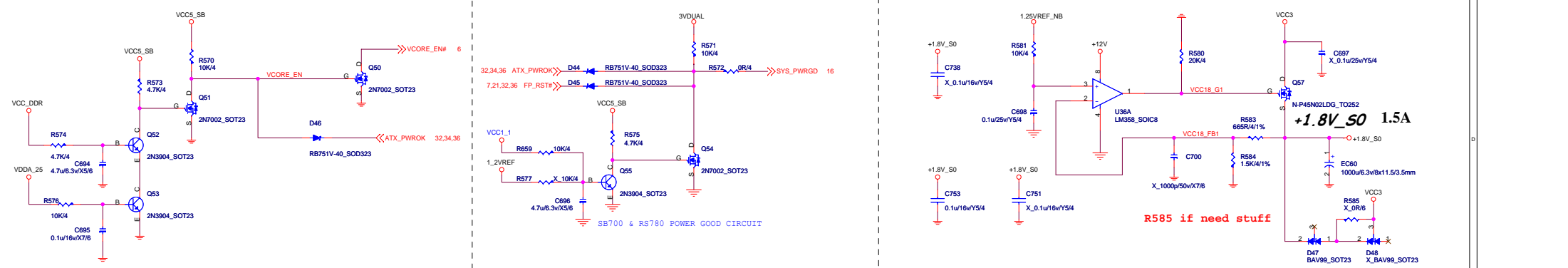
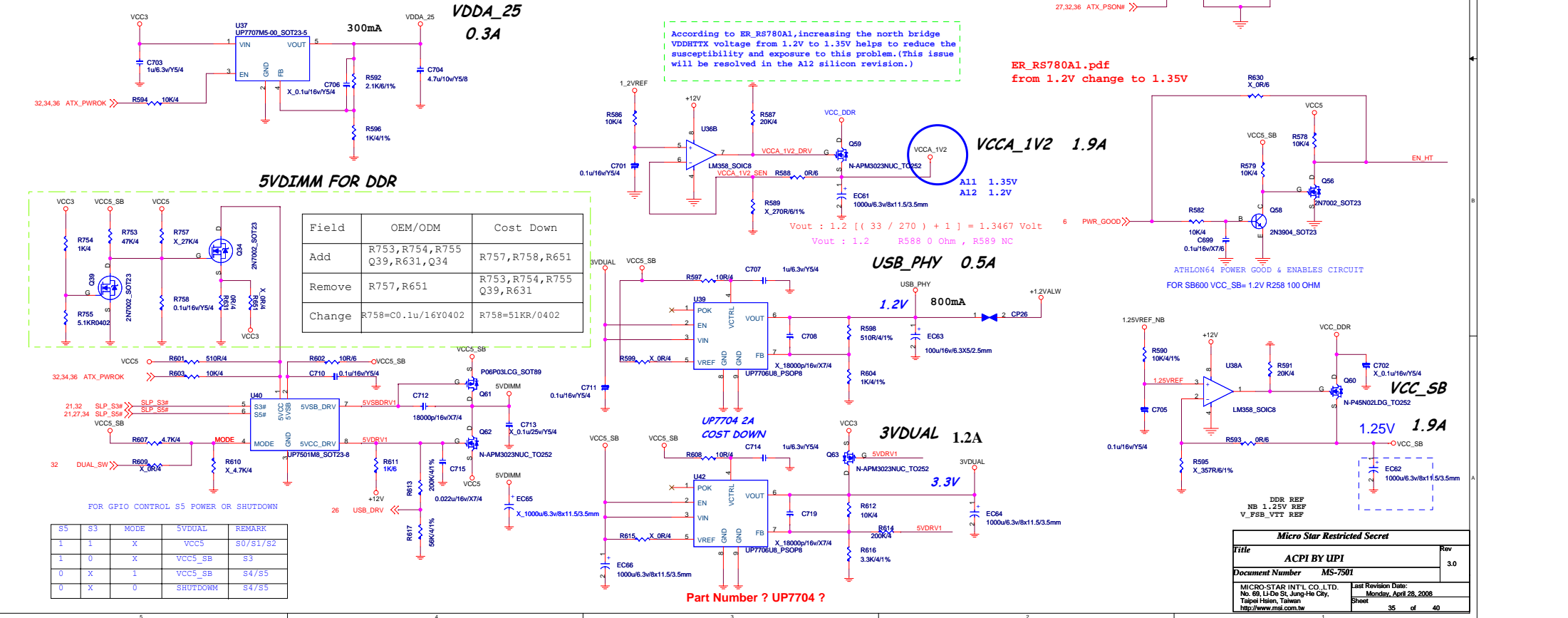


Table 15. Power Sequencing Group Definitions

Power Group A	Power Group B
VDDIO ^{1,2} Vcc_DDR	VDD[1:0] ³ Vcore
VTT ^{1,2} VTT	VDDNB Vcore_NB
VDDA VDDA25	VLDT HT

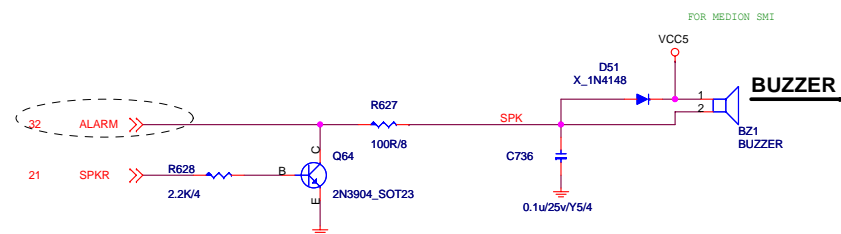
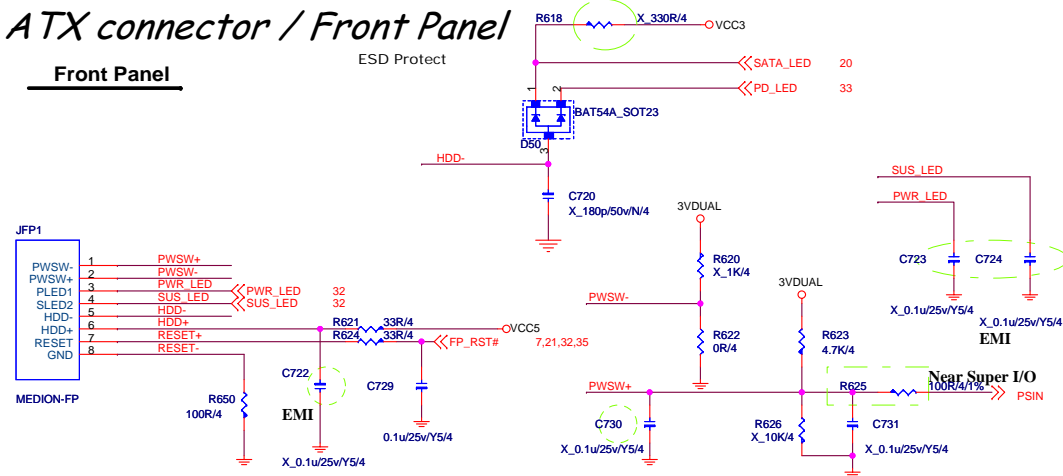
Notes:

- 1) VDDIO must never exceed VTT by greater than X.XX V. This relationship must be enforced at all times including power-up, power-down, and power failure.
- 2) VDDIO and VTT only apply to DDR2 compatible processors.
- 3) VDD refers generically to the core voltage plane(s). VDD0 refers to processor power plane 0, and VDD1 refers to processor power plane 1.

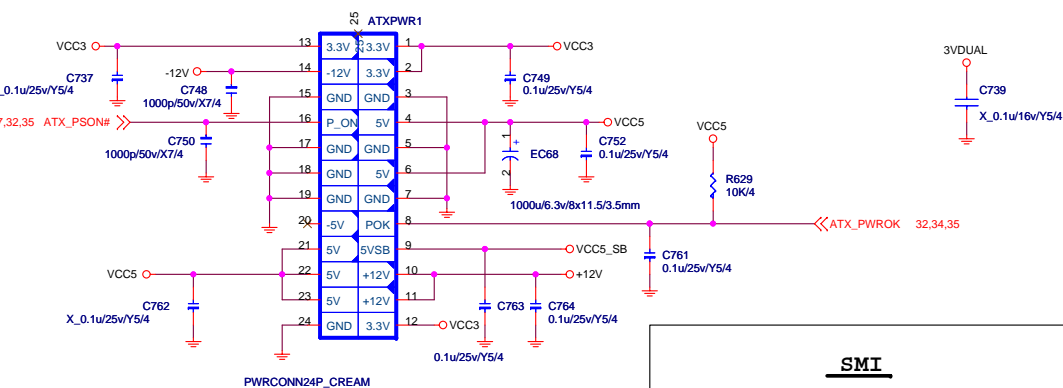


ATX connector / Front Panel

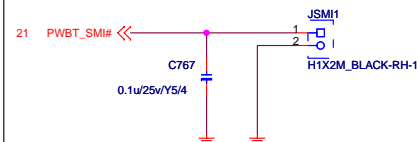
Front Panel



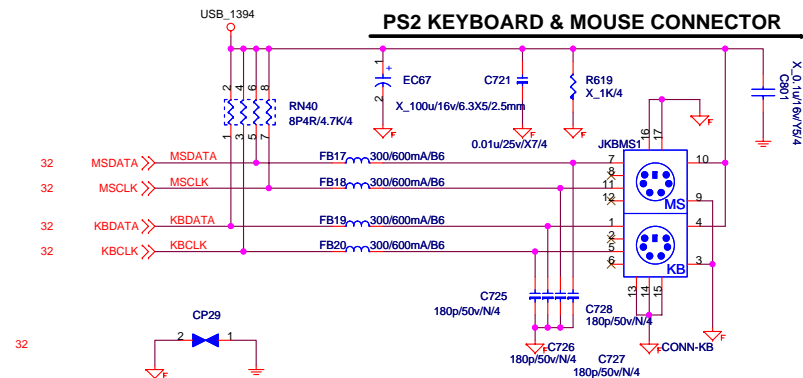
ATX Connector



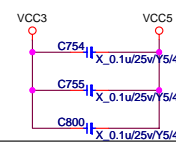
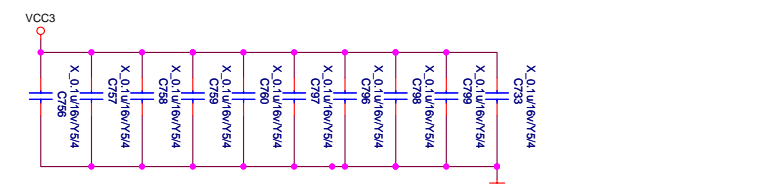
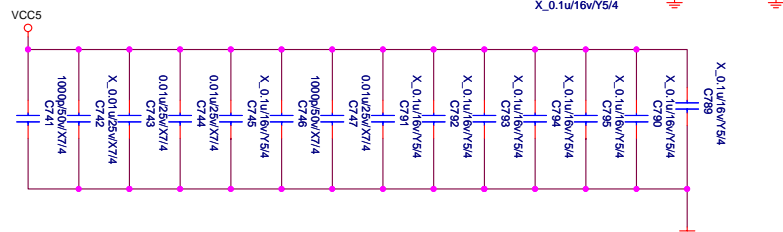
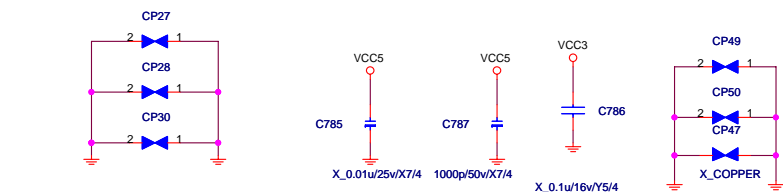
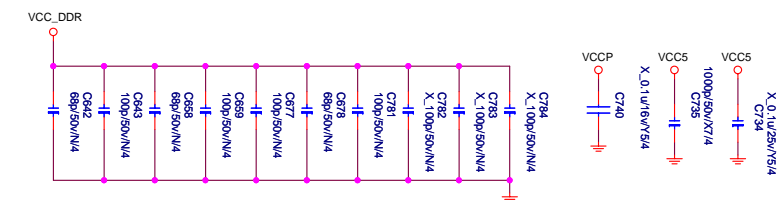
SMI



PS2 KEYBOARD & MOUSE CONNECTOR

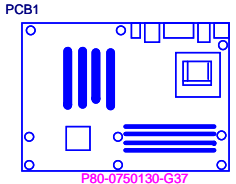


EMI solution



Micro Star Restricted Secret			
Title ATX/Front Panel/KB/EMI			Rev 3.0
Document Number MS-7501			
MICRO-STAR INT'L CO. LTD. No. 69, Li-De St, Jung-Hei City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, April 28, 2008 Sheet <div style="display: flex; justify-content: space-between;"> 36 of 40 </div>	

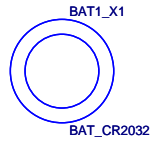
PCB



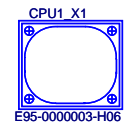
PCB : 2116

P80-0750130-G37
P80-0750130-E55

BATTERY



CPU RM

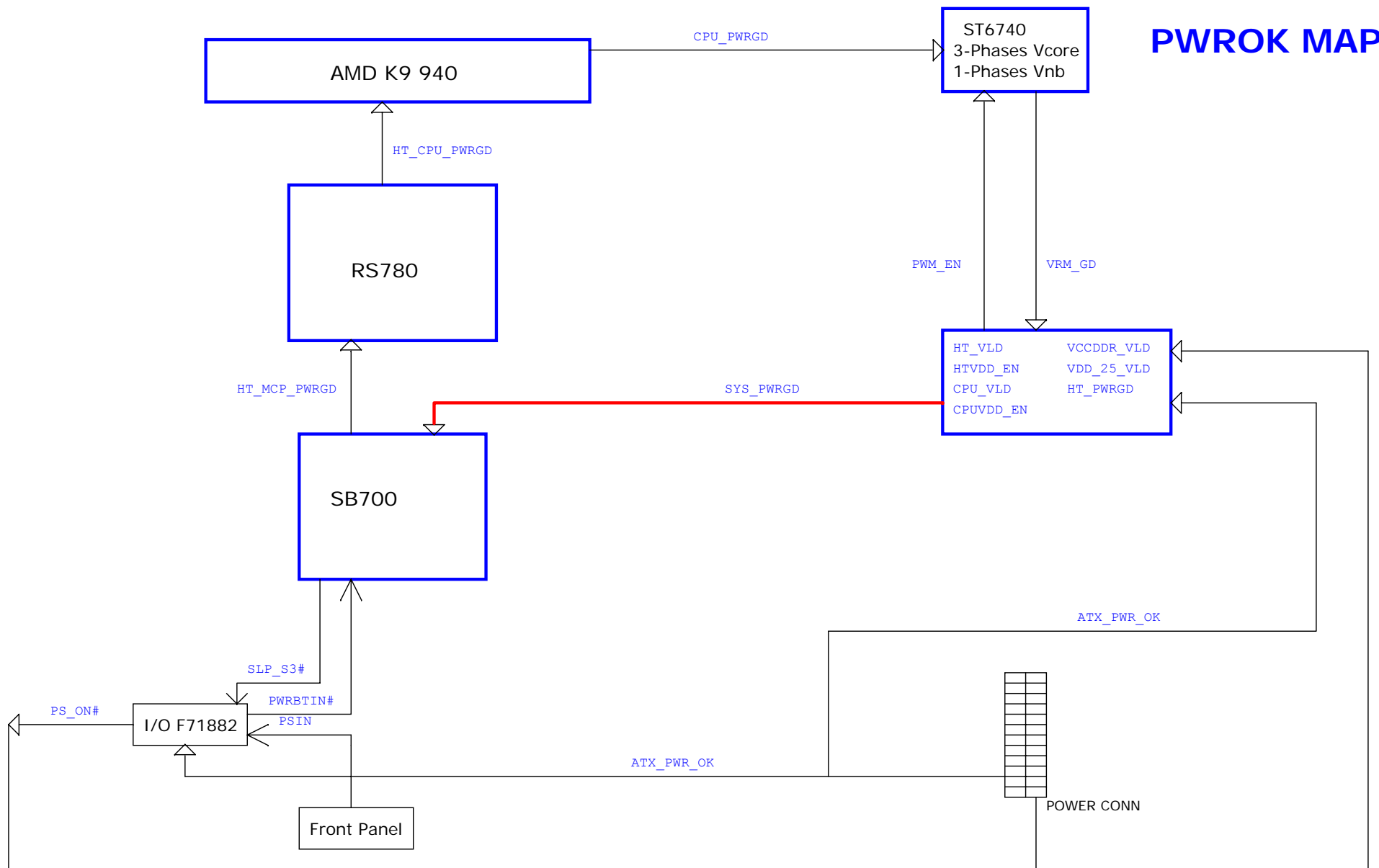


RS780M

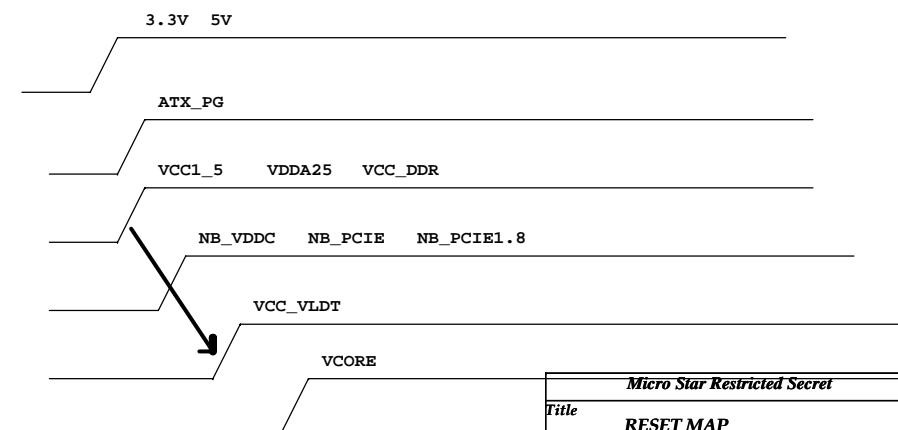
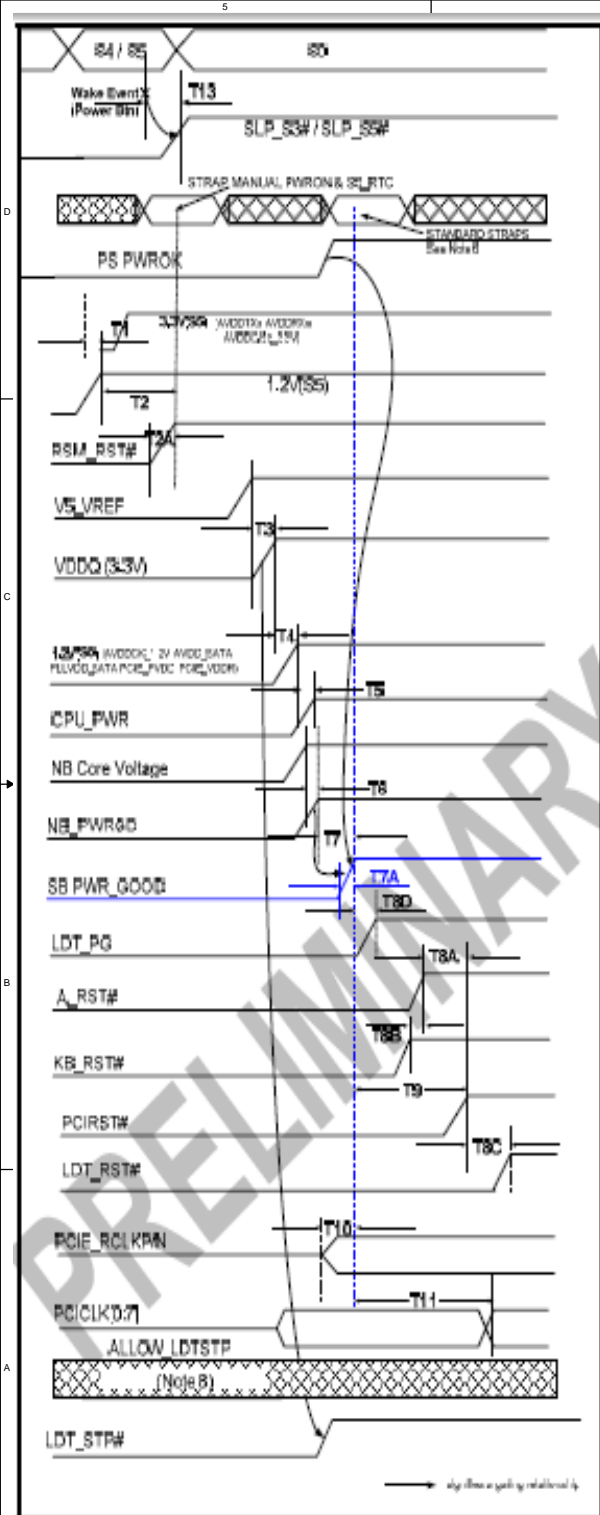


U10 & U13 new version (Part number) ?

MICRO-STAR INT'L CO., LTD.			
Title BOM - Option Parts			
Size	Document Number		Rev
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PWROK MAP



Micro Star Restricted Secret		
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1. BOM

Ver.	Description	P/N	OPT	CFG
0A	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888+JMB381+ICS9LPRS477	601-7501-A10		CFG_7501
2.0	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888+JMB381+ICS9LPRS477	601-7501-01S		CFG_7501
2.1	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888+JMB381+ICS9LPRS477	601-7501-04S		CFG_7501
2.1	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888S-VC +VT6308+88SE6111	601-7501-05S	SVC	CFG_7501
3.0	RS780+SB700+ST6740L+F71882+RTL8111C +ALC888S-VC+VT6308+88SE6111			CFG_7501
3.0	RS780M +SB700+ST6740L+F71882+RTL8111C +ALC888S-VC+VT6308+88SE6111		M	CFG_7501M

2.Modify list

7501-2.0

- 1.修改為Medion所要的相關connector規格
- 2.Modify NB heatsink
- 3.Add sata 5 and sata6

7501-3.0

OPT:M

- 1.Modify NB CHIP TO RS780M

7501-2.1

- 1.Modify SATA connector 為90度
- 2.Modify FAN circuit

7501-2.1

OPT:SVC

- 1.Modify Audio為ALC888S-VC
- 2.Remove HDMI and VGA

7501-3.0

- 1.Modify PWM為5相

Micro Star Restricted Secret		
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MICRO-STAR INT'L CO.,LTD. No. 68, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Monday, April 28, 2008 Sheet 40 of 40